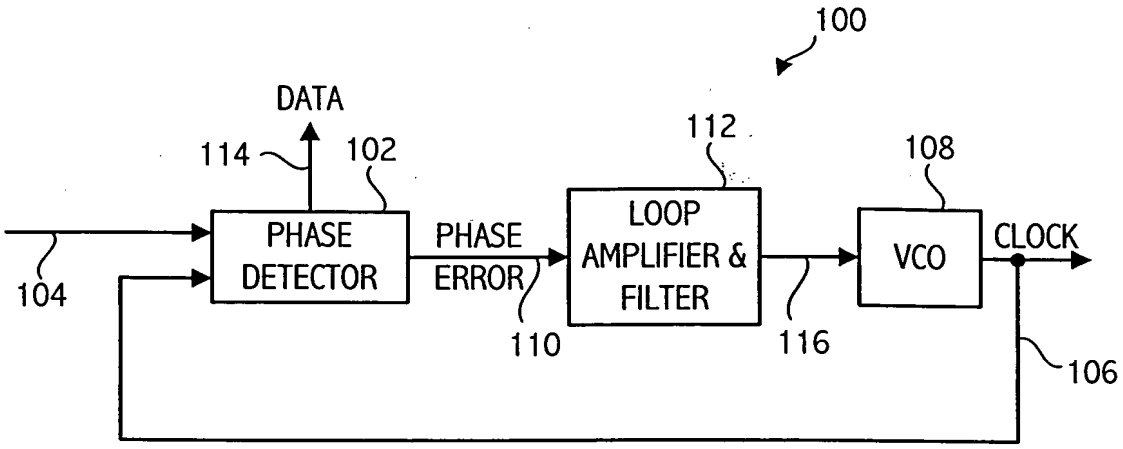
100
DATA
114
102
112
108
PHASE
DETECTOR
PHASE
ERROR
LOOP
AMPLIFIER &
FILTER
VCO
CLOCK
104
110
116
106

FIG. 1

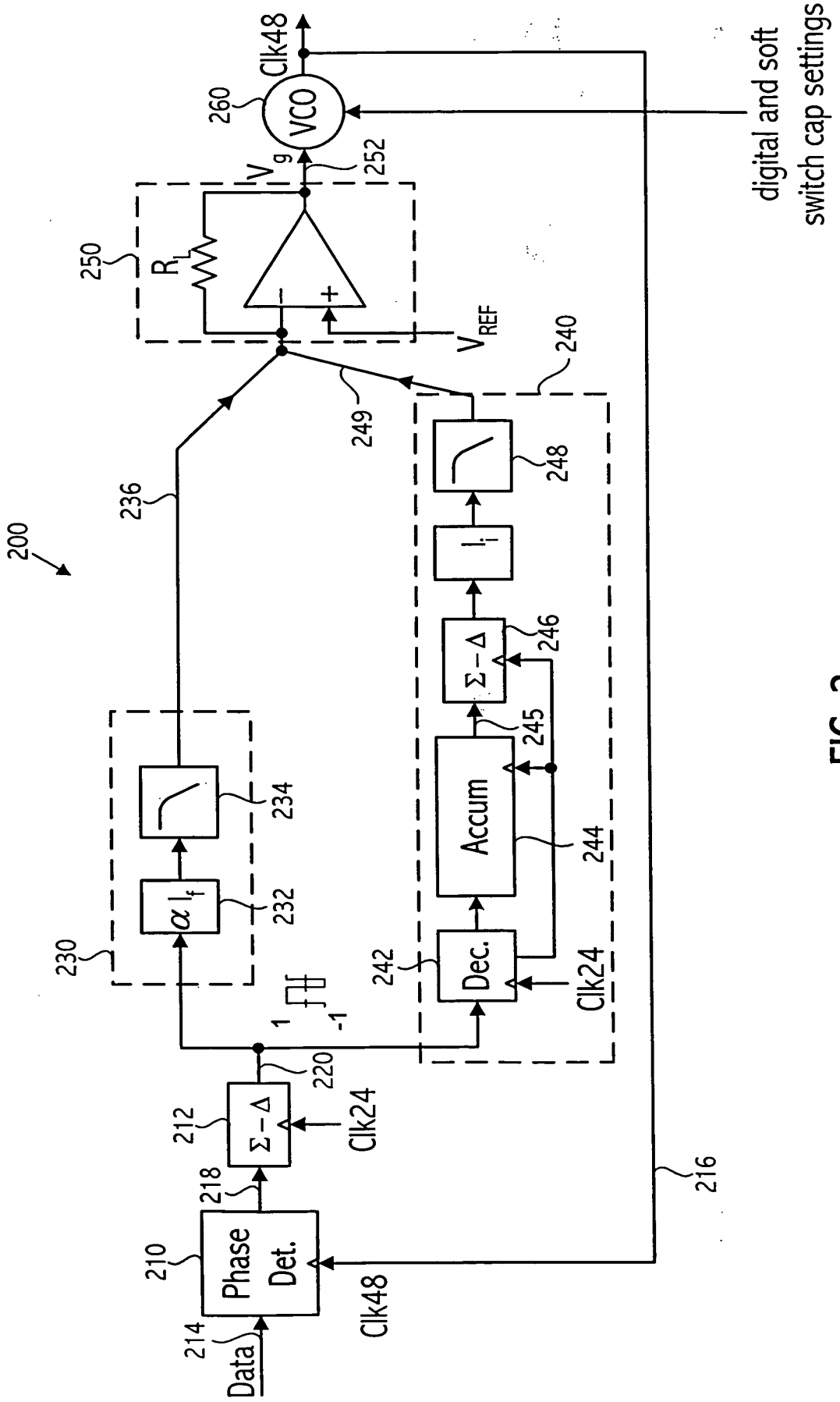
200
Clk48
260
VCO
V_g
252
250
R_L
V_{REF}
digital and soft
switch cap settings
240
249
248
236
I_i
246
$\Sigma-\Delta$
245
Accum
244
234
αI_f
232
230
242
Dec.
Clk24
1
f_s
-1
220
212
$\Sigma-\Delta$
Clk24
218
210
Phase
Det.
214
Data
Clk48
216

FIG. 2

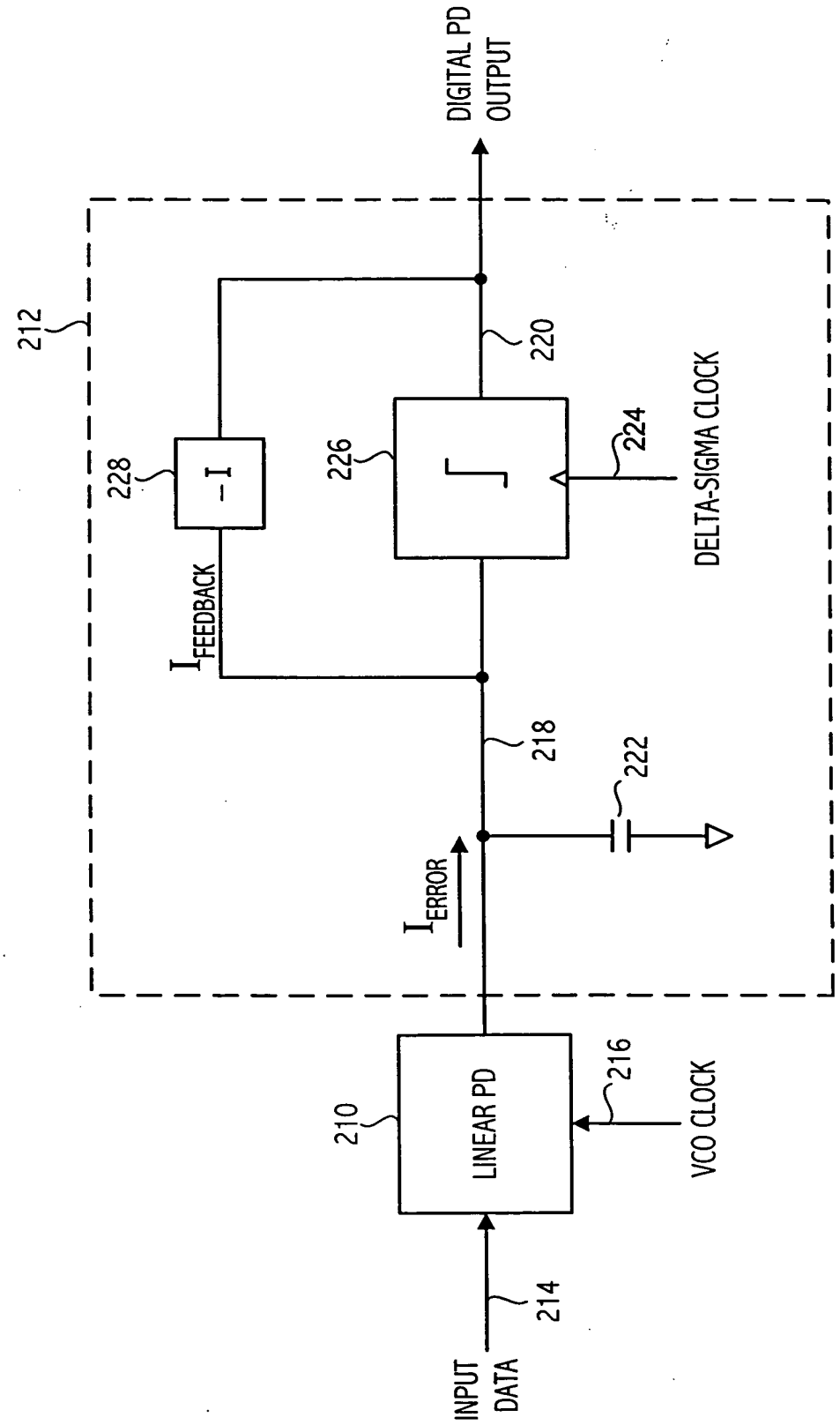
202
DIGITAL PD OUTPUT
212
220
226
224
DELTA-SIGMA CLOCK
228
-I
$I_{FEEDBACK}$
218
222
I_{ERROR}
210
LINEAR PD
216
VCO CLOCK
214
INPUT DATA

FIG. 3

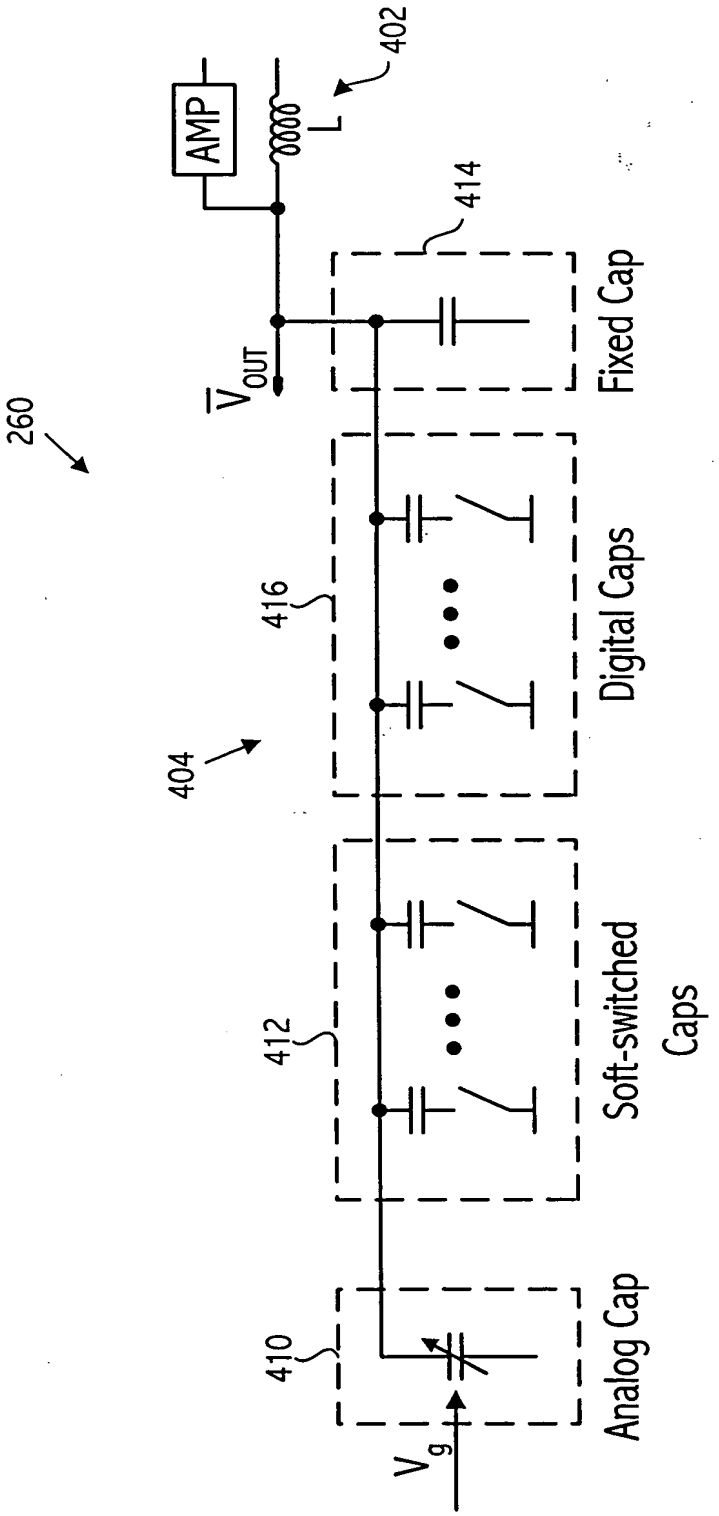
260
AMP
402
L
414
Fixed Cap
V_{OUT}
404
416
Digital Caps
412
Soft-switched
Caps
410
Analog Cap
V_g

FIG. 4A

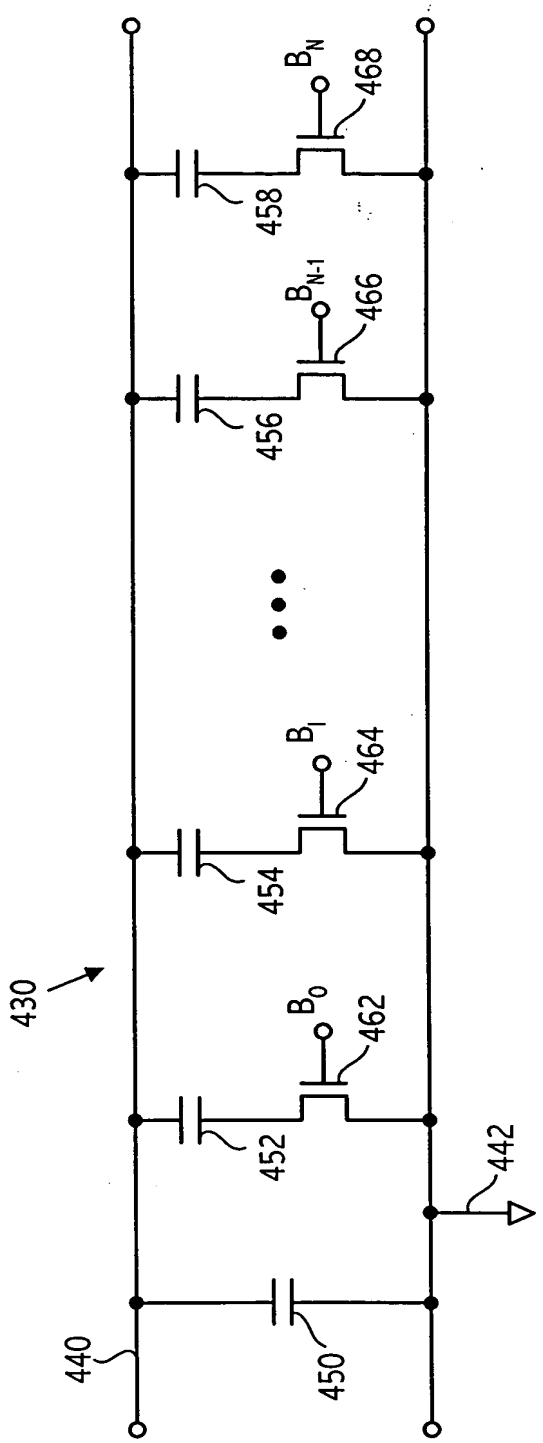

FIG. 4B

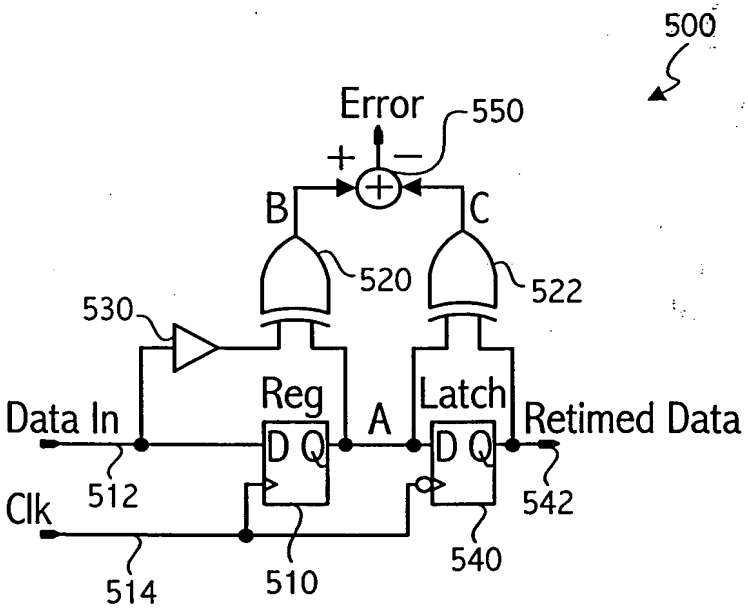
500
Error
550
+
−
B
C
520
522
530
Reg
Latch
Data In
A
Retimed Data
D Q
D Q
512
542
Clk
540
514
510

FIG. 5

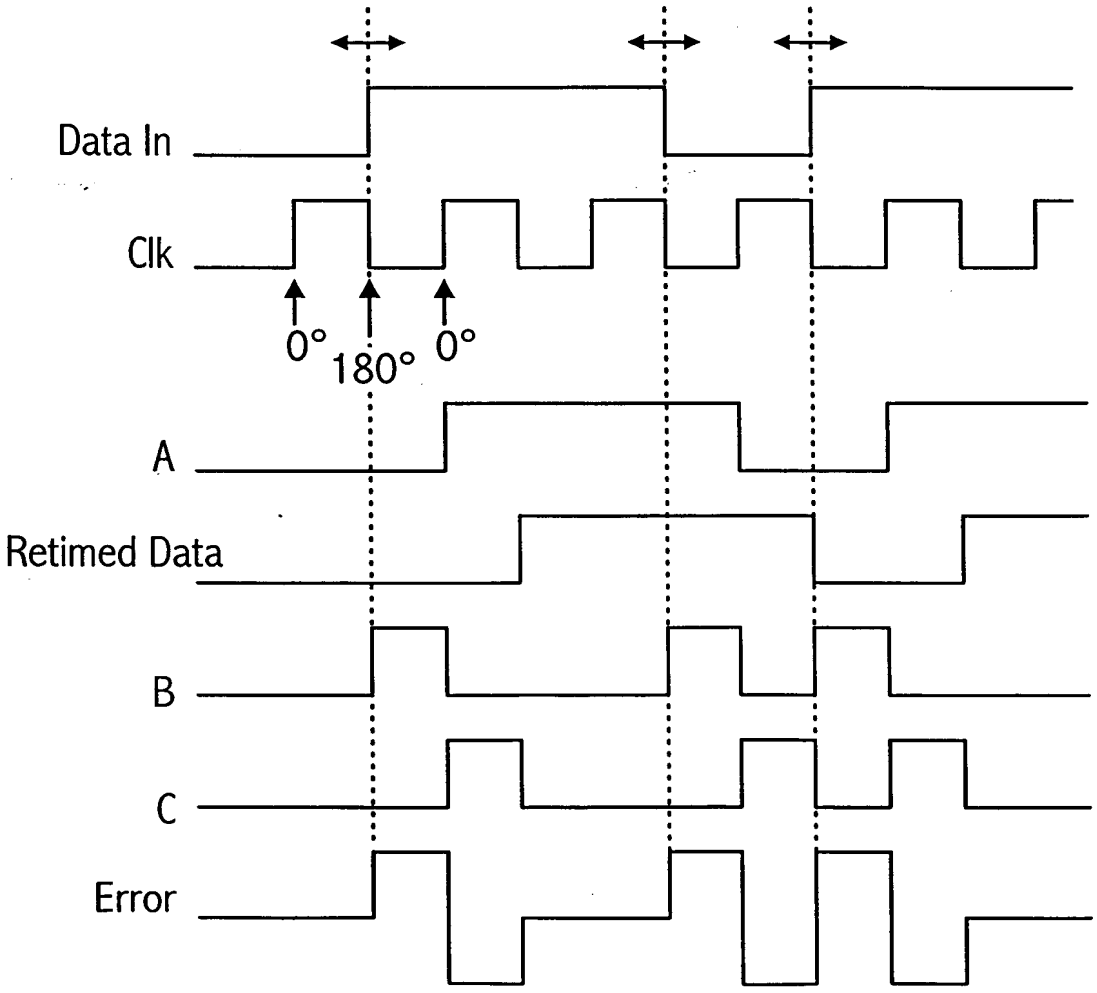
Data In
Clk
0°
180°
0°
A
Retimed Data
B
C
Error

FIG. 6

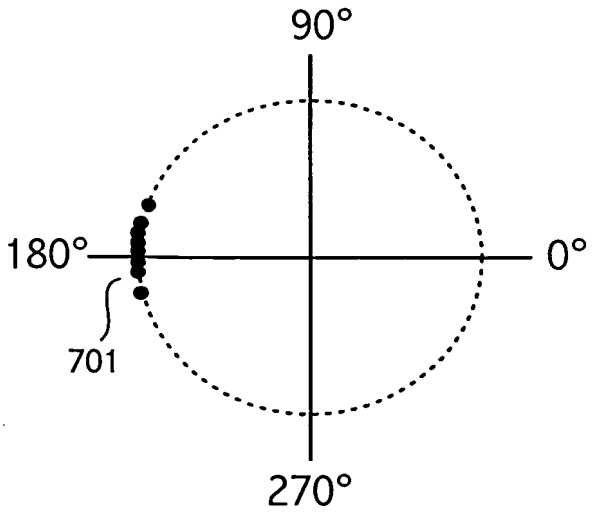

FIG. 7

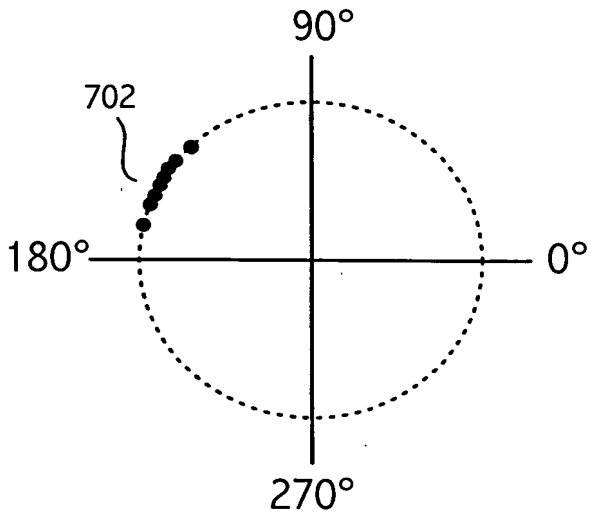

FIG. 8

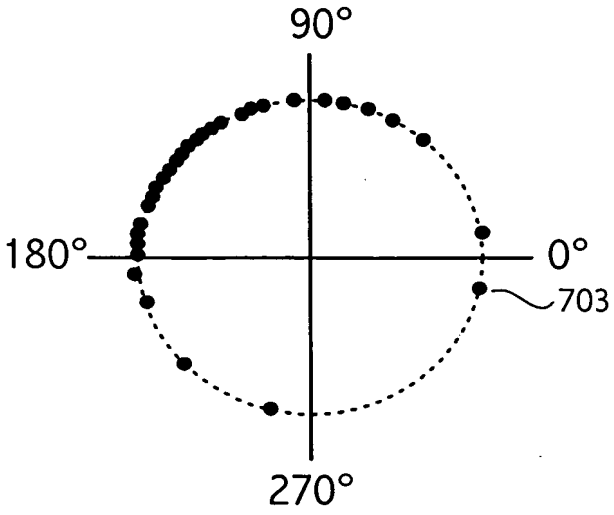

FIG. 9

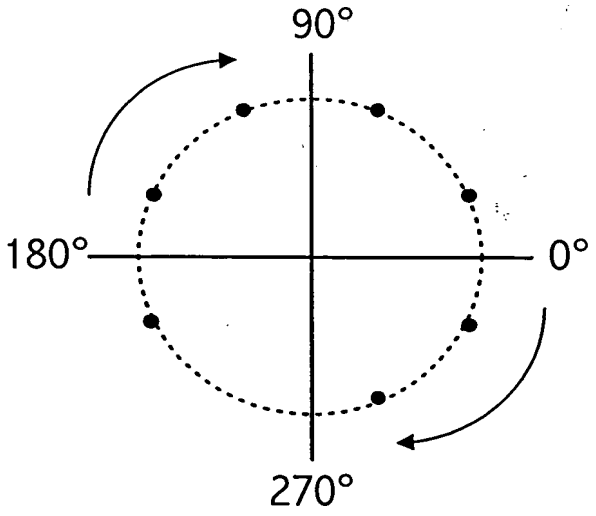

FIG. 10

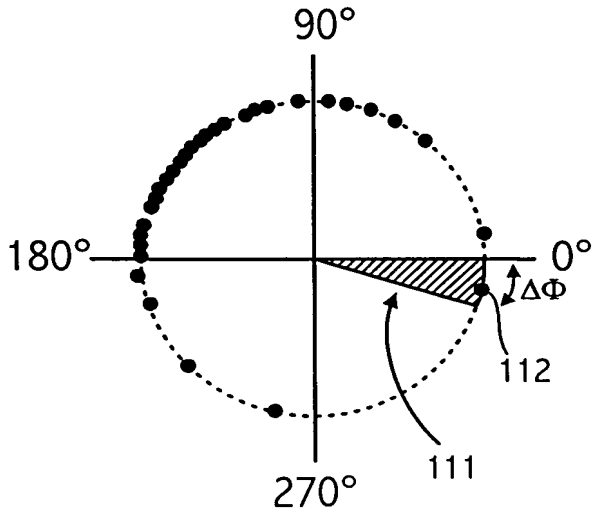

FIG. 11

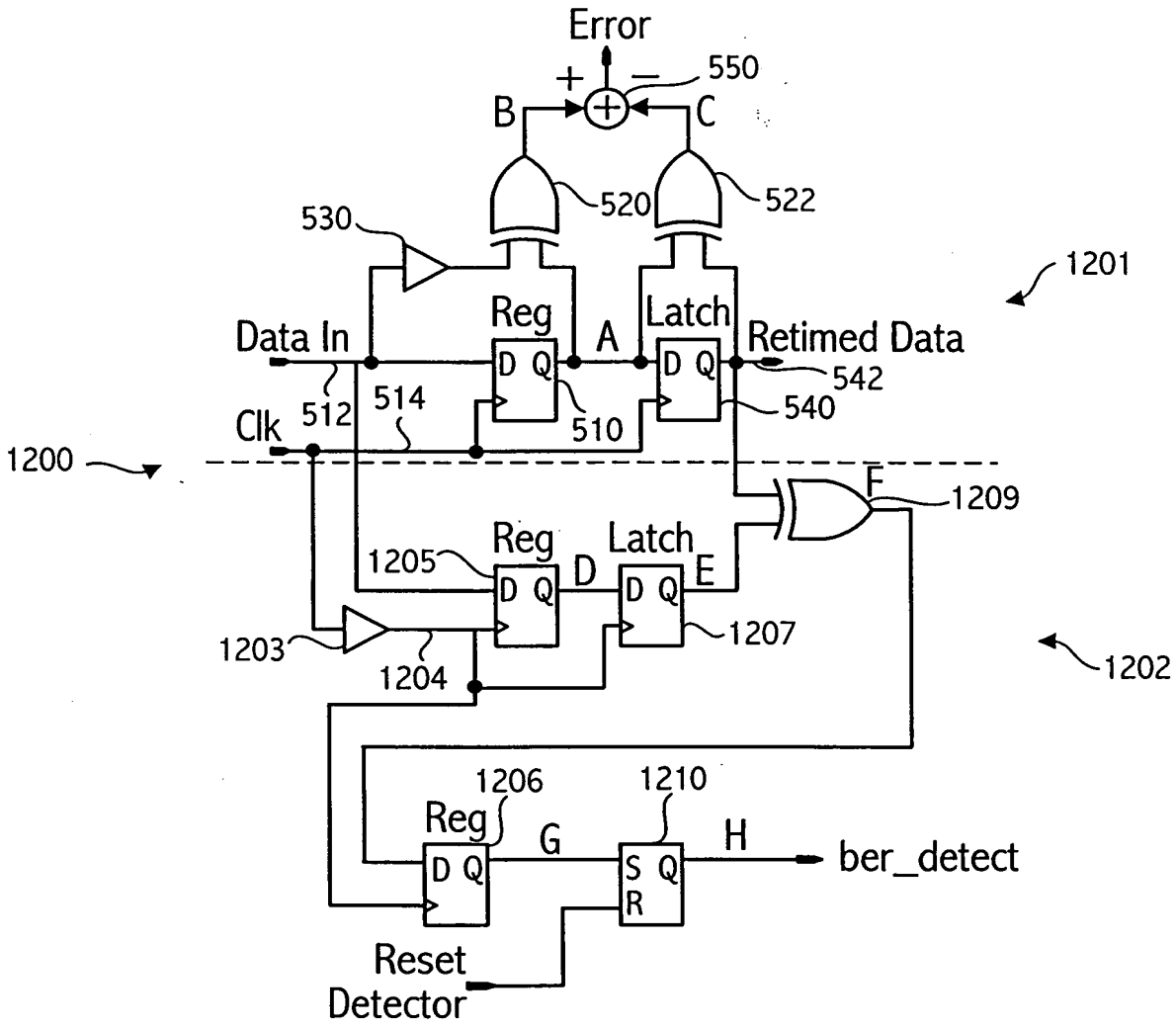
Error
+
−
550
B
C
520
522
530
1201
Reg
A
Latch
Data In
D Q
D Q
Retimed Data
542
514
512
510
540
Clk
1200
F
1209
Reg
Latch
1205
D
E
D Q
D Q
1207
1203
1204
1202
1206
1210
Reg
G
H
D Q
S Q
R
ber_detect
Reset
Detector

FIG. 12A

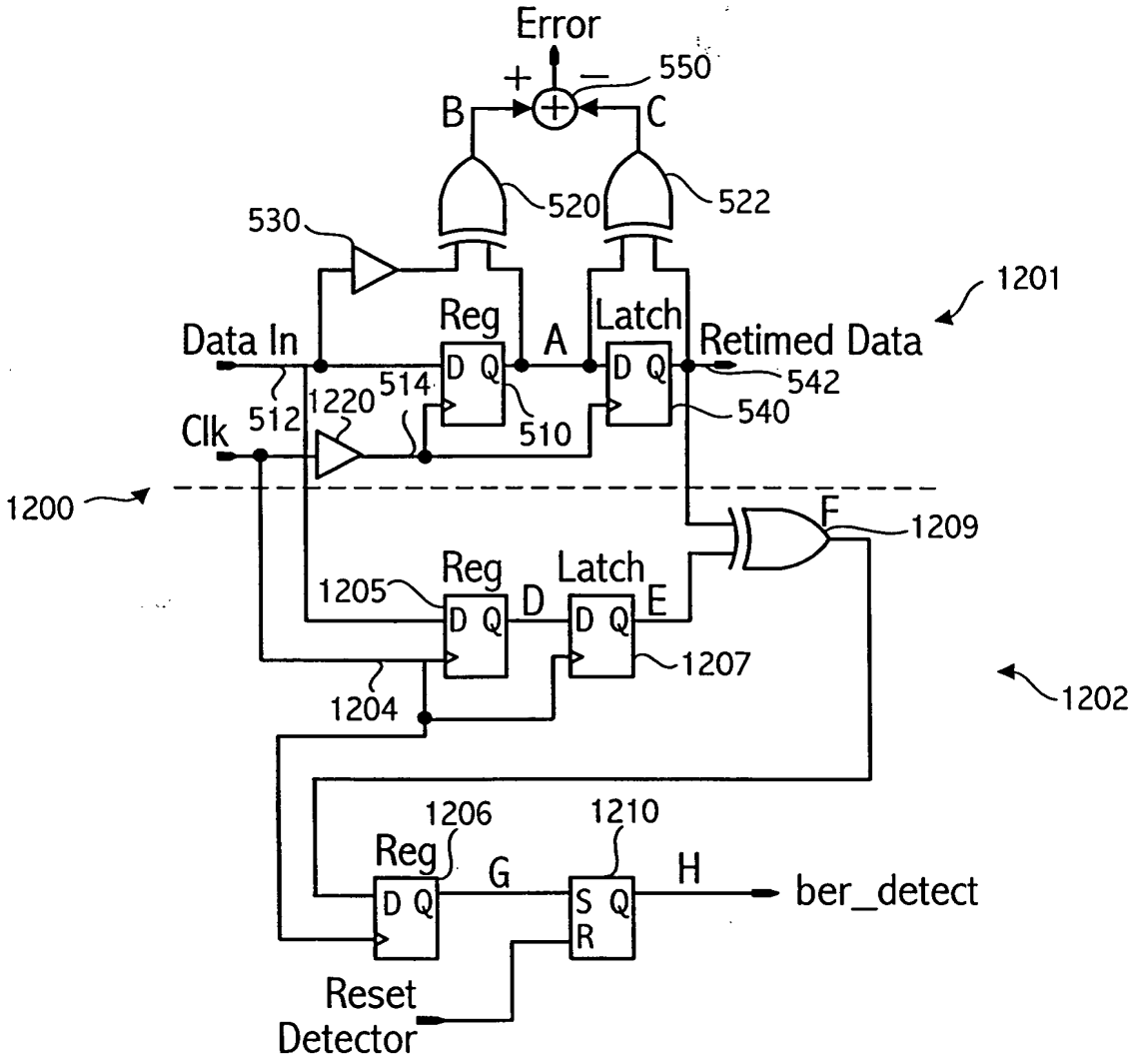
Error
+
−
550
B
C
520
522
530
1201
Reg
A
Latch
Data In
Retimed Data
D Q
D Q
542
514
1220
512
510
540
Clk
1200
F
1209
Reg
Latch
1205
D
E
D Q
D Q
1207
1204
1202
1206
1210
Reg
G
H
ber_detect
D Q
S Q
R
Reset
Detector

FIG. 12B

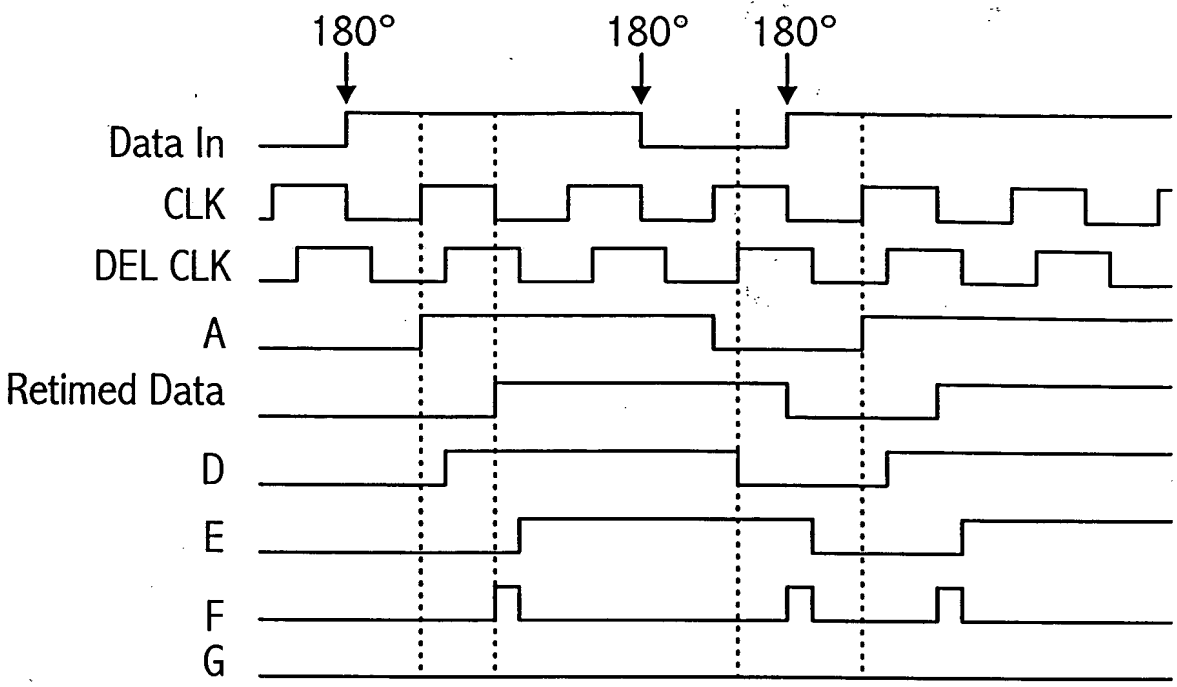

FIG. 13A

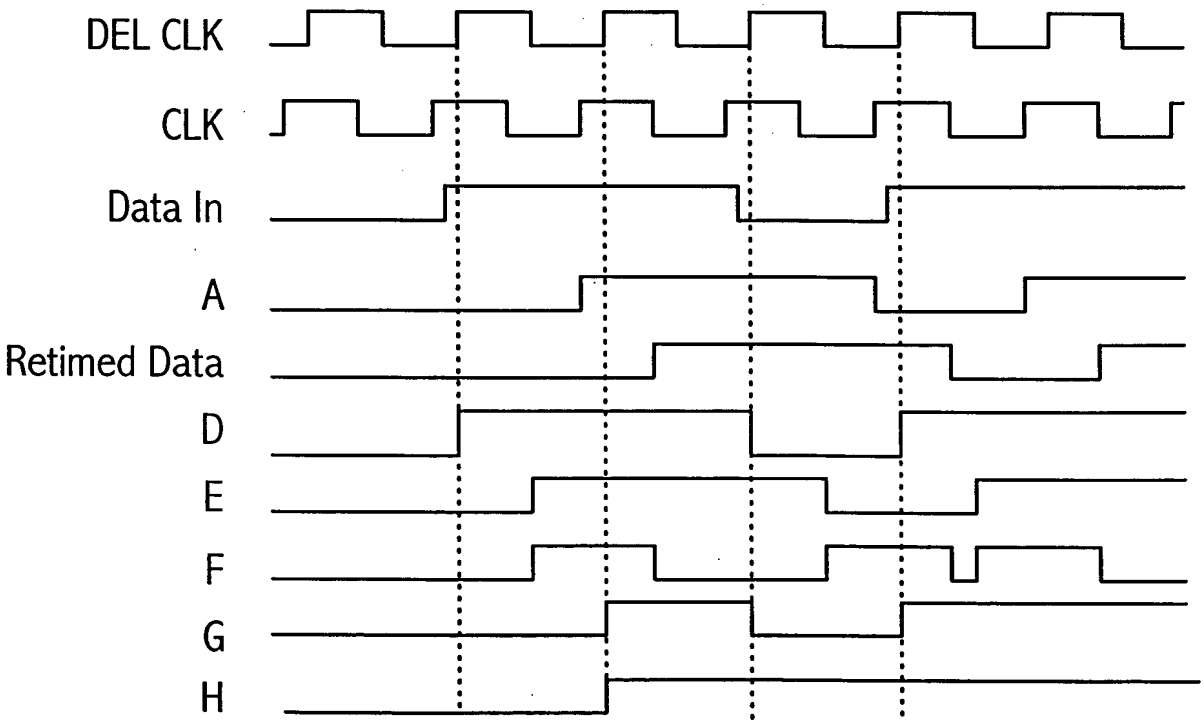

FIG. 13B

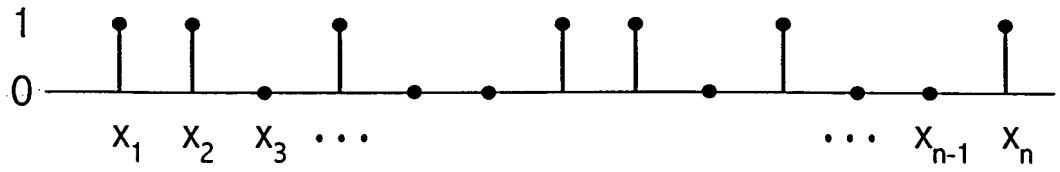

FIG. 14

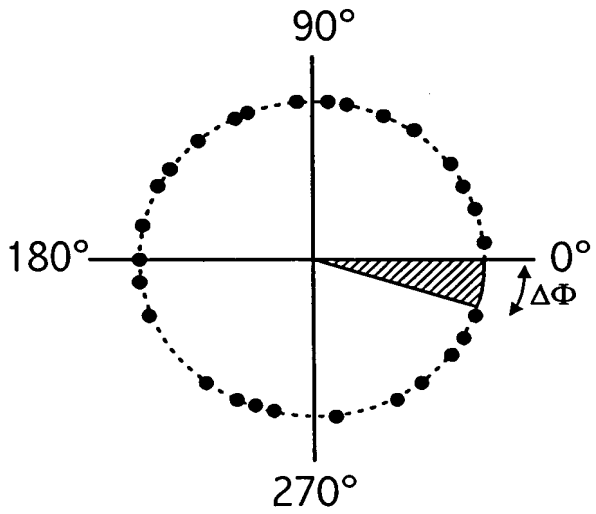

FIG. 15

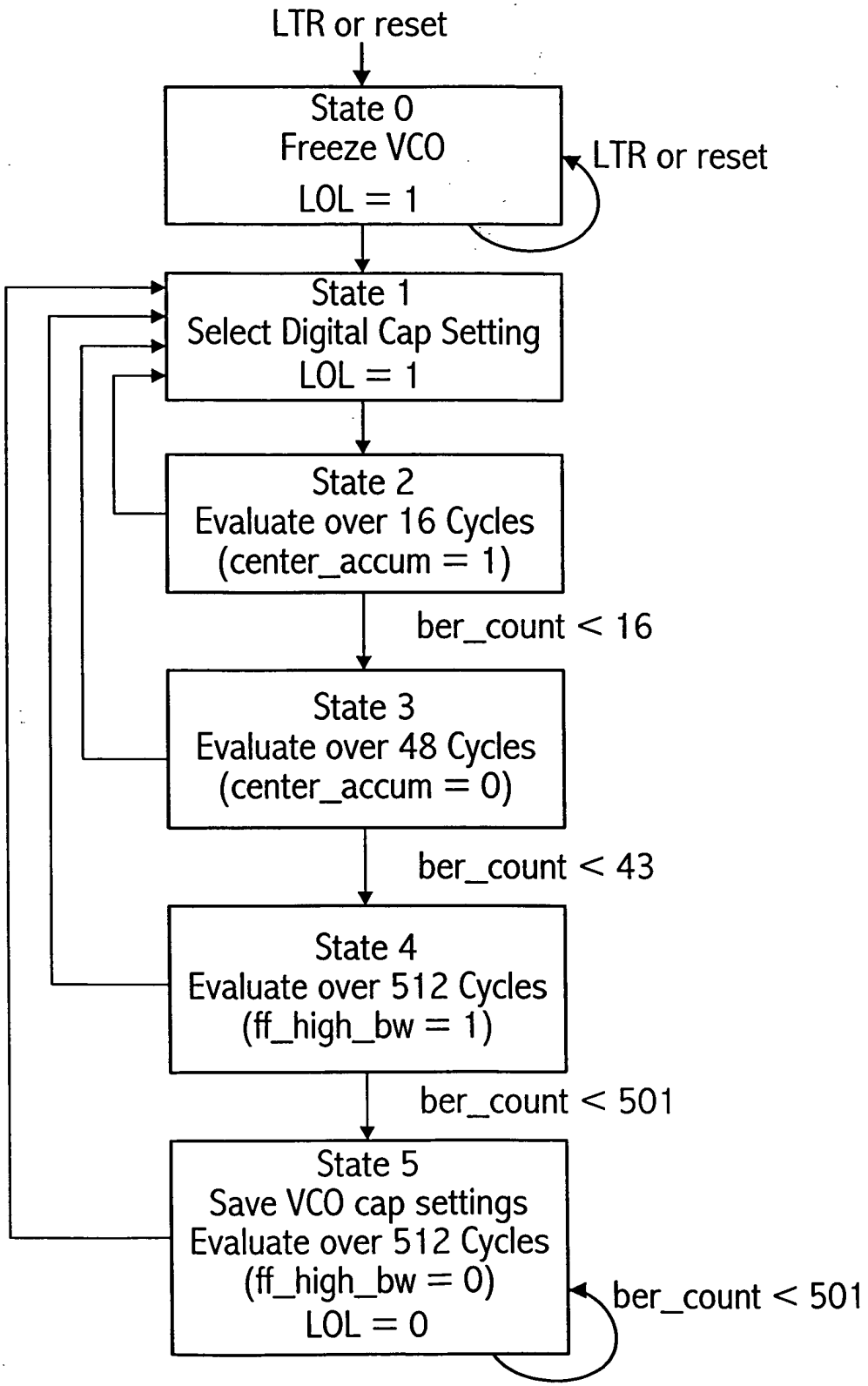
LTR or reset
State 0
Freeze VCO
LOL = 1
LTR or reset
State 1
Select Digital Cap Setting
LOL = 1
State 2
Evaluate over 16 Cycles
(center_accum = 1)
ber_count < 16
State 3
Evaluate over 48 Cycles
(center_accum = 0)
ber_count < 43
State 4
Evaluate over 512 Cycles
(ff_high_bw = 1)
ber_count < 501
State 5
Save VCO cap settings
Evaluate over 512 Cycles
(ff_high_bw = 0)
LOL = 0
ber_count < 501

FIG. 16

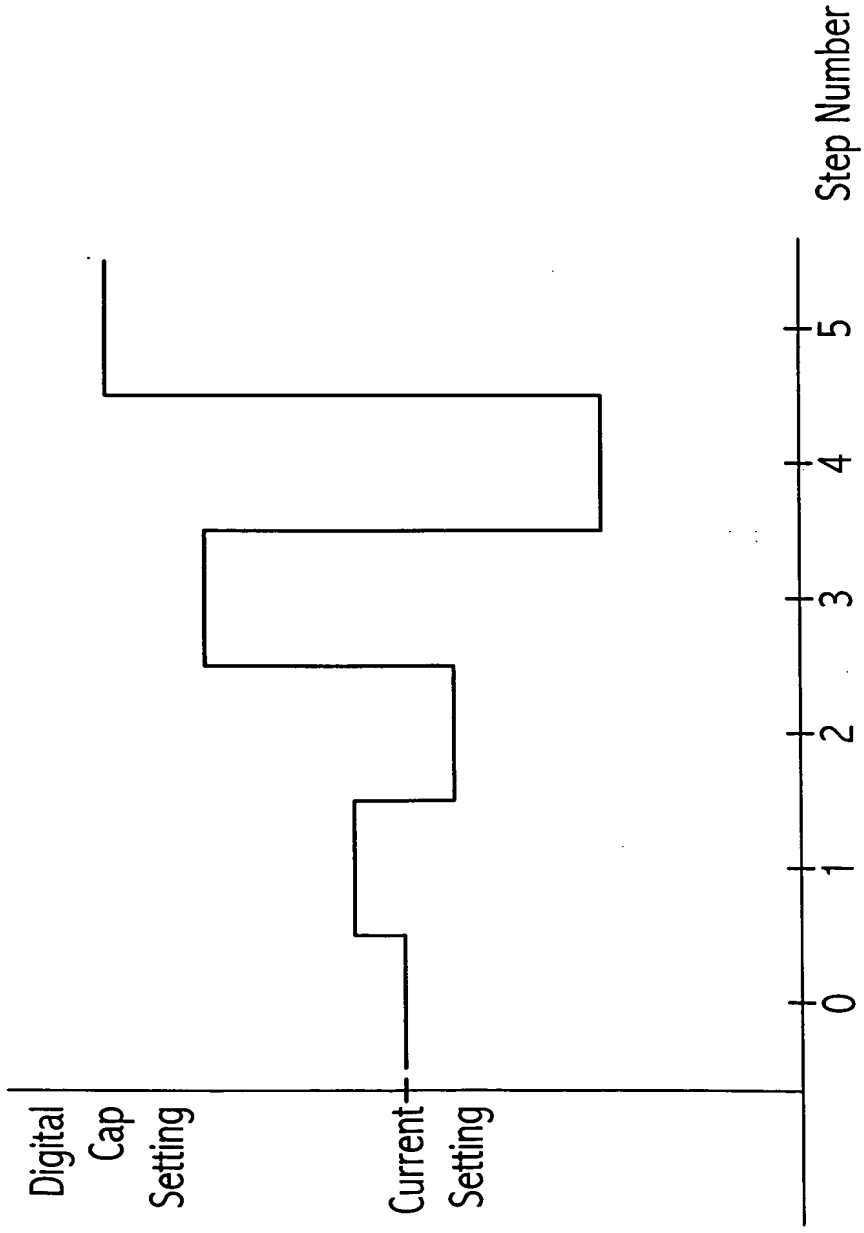

FIG. 17

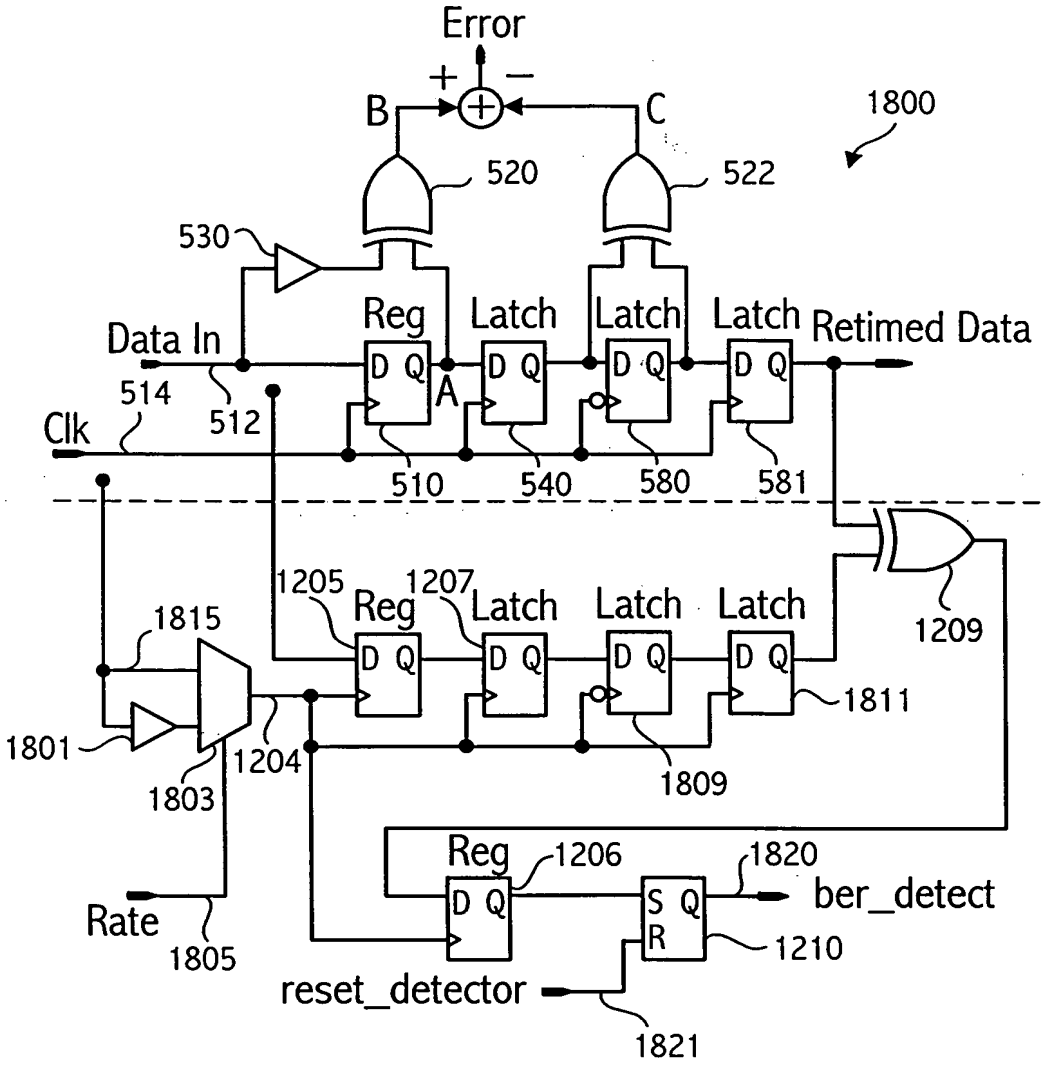
Error
+
−
B
C
1800
520
522
530
Reg
Latch
Latch
Latch
Retimed Data
Data In
D Q
A
514
512
Clk
510
540
580
581
1205
1207
Reg
Latch
Latch
Latch
1209
1815
1811
1801
1204
1803
1809
Reg
1206
1820
ber_detect
Rate
1805
S Q
R
1210
reset_detector
1821

FIG. 18

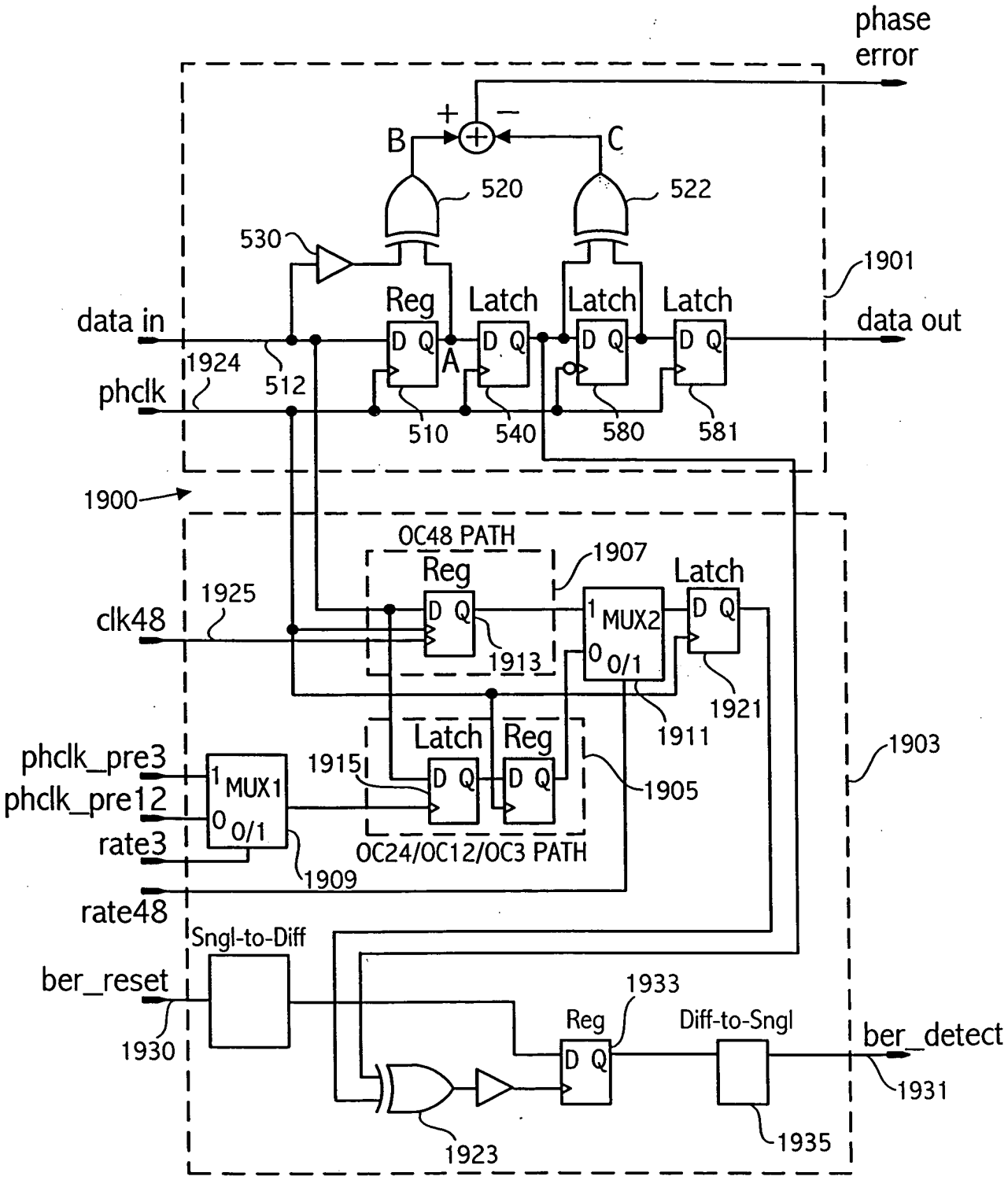
phase error
+
−
B
C
520
522
530
1901
Reg
Latch
Latch
Latch
data in
data out
D Q
A
1924
512
phclk
510
540
580
581
1900
OC48 PATH
1907
Reg
Latch
1925
clk48
MUX2
1913
1921
1911
Latch
Reg
1903
phclk_pre3
phclk_pre12
rate3
MUX1
1915
1905
OC24/OC12/OC3 PATH
1909
rate48
Sngl-to-Diff
ber_reset
1933
Reg
Diff-to-Sngl
ber_detect
1930
1931
1923
1935

FIG. 19

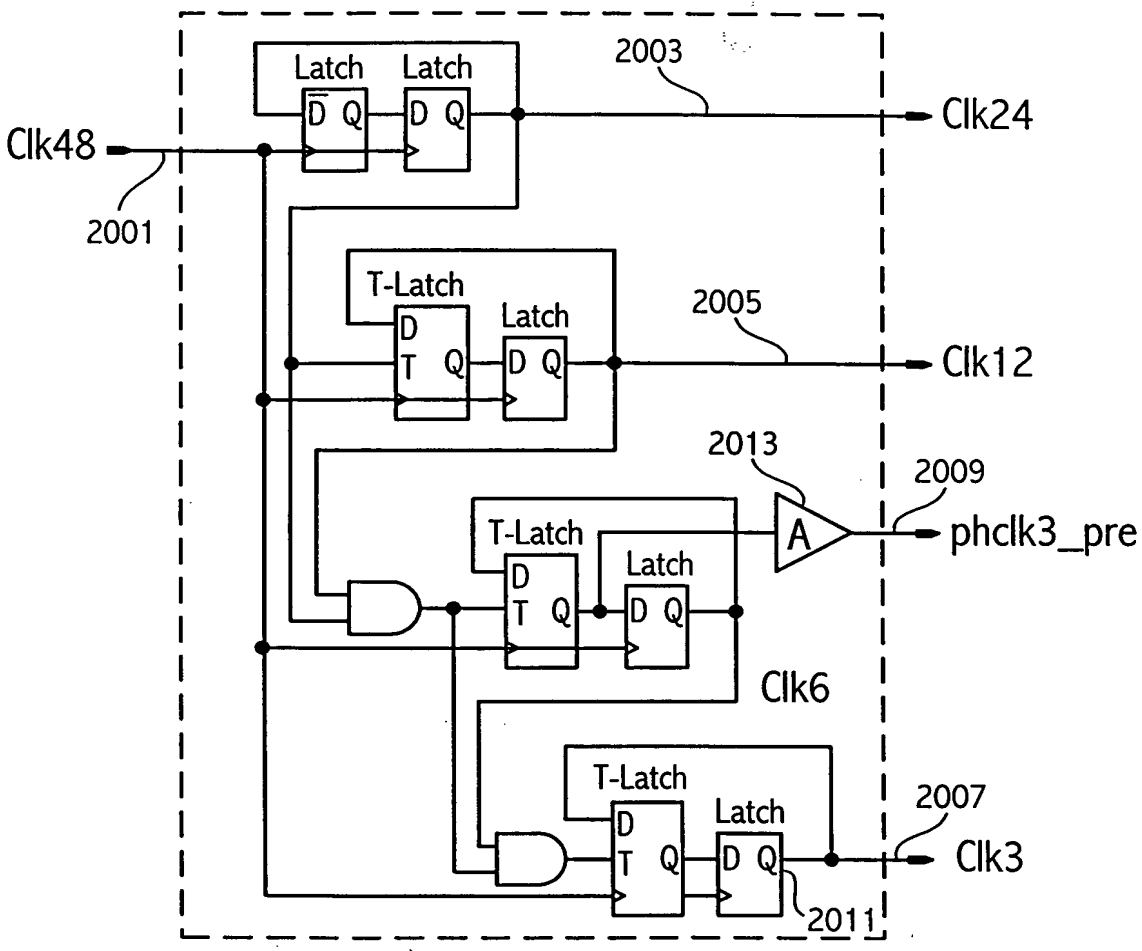
Clk48
2001
Latch
Latch
D Q
D Q
2003
Clk24
T-Latch
D
T Q
Latch
D Q
2005
Clk12
2013
2009
A
phclk3_pre
T-Latch
D
T Q
Latch
D Q
Clk6
T-Latch
D
T Q
Latch
D Q
2007
Clk3
2011

FIG. 20

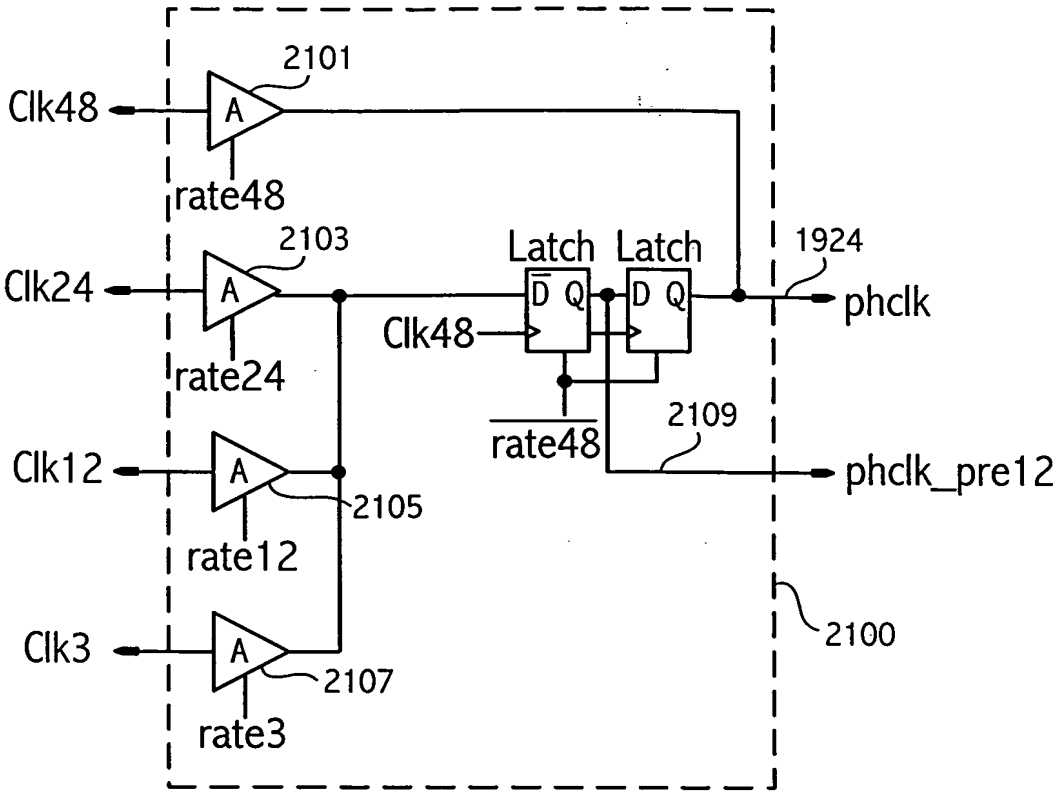
2101
Clk48
A
rate48
2103
Clk24
A
rate24
Latch
Latch
1924
D Q
D Q
phclk
Clk48
2109
rate48
Clk12
A
2105
rate12
phclk_pre12
Clk3
A
2107
rate3
2100

FIG. 21

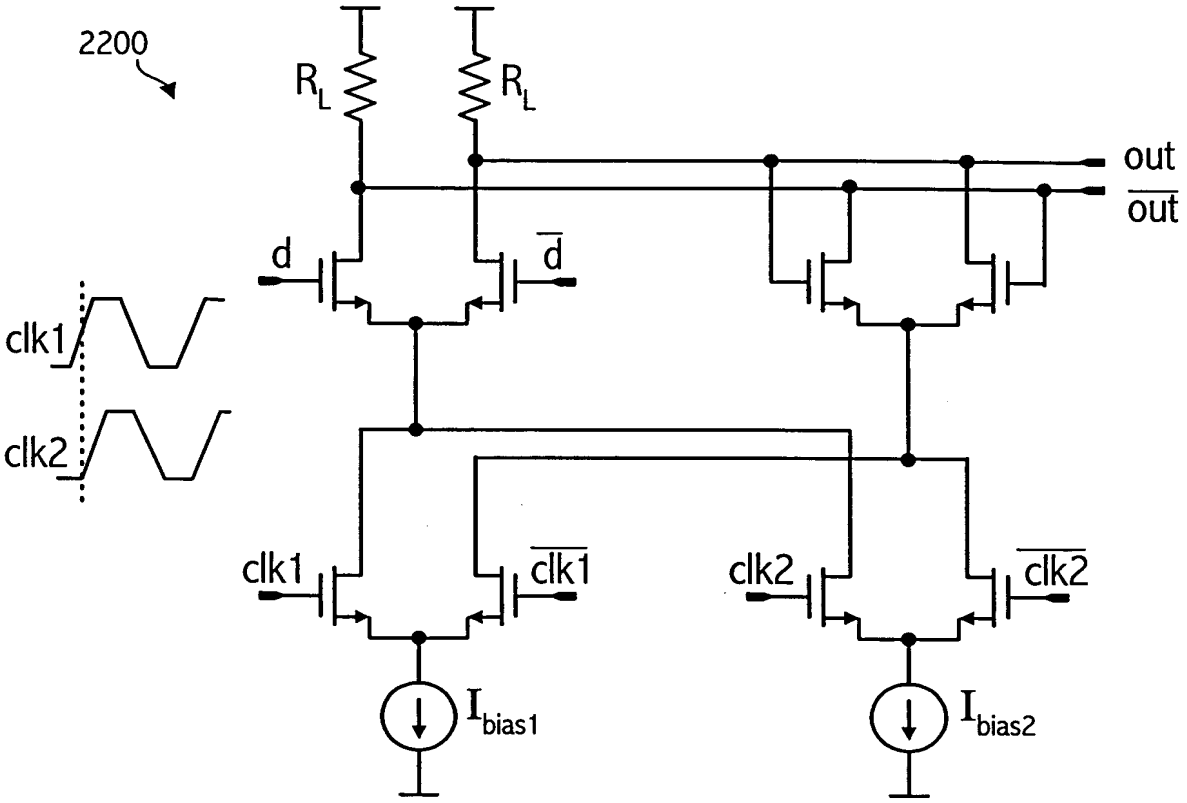
2200
R_L
R_L
out
$\overline{out}$
d
$\overline{d}$
clk1
clk2
clk1
$\overline{clk1}$
clk2
$\overline{clk2}$
I_{bias1}
I_{bias2}

FIG. 22

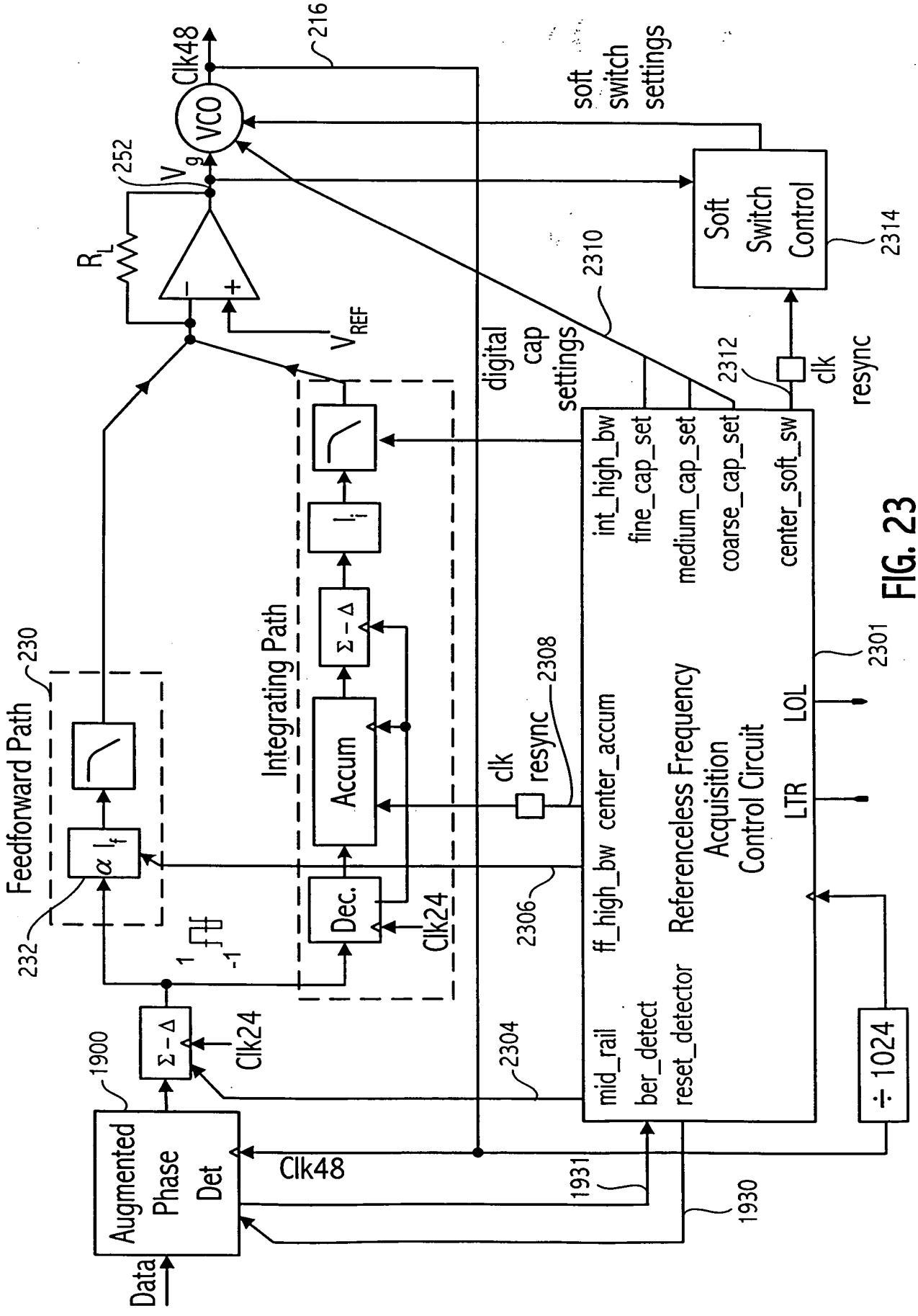
Clk48
VCO
216
soft switch settings
252
V_g
R_L
V_{REF}
Soft Switch Control
2314
2310
digital cap settings
2312
clk resync
int_high_bw
fine_cap_set
medium_cap_set
coarse_cap_set
center_soft_sw
Feedforward Path
230
Integrating Path
α I_f
I_i
Σ - Δ
Accum
Dec.
clk resync
2308
2306
Clk24
232
$\frac{1}{1-z^{-1}}$
ff_high_bw
center_accum
Referenceless Frequency Acquisition Control Circuit
2301
LOL
LTR
mid_rail
ber_detect
reset_detector
2304
1900
Augmented Phase Det
Clk48
÷ 1024
1931
1930
Data

FIG. 23

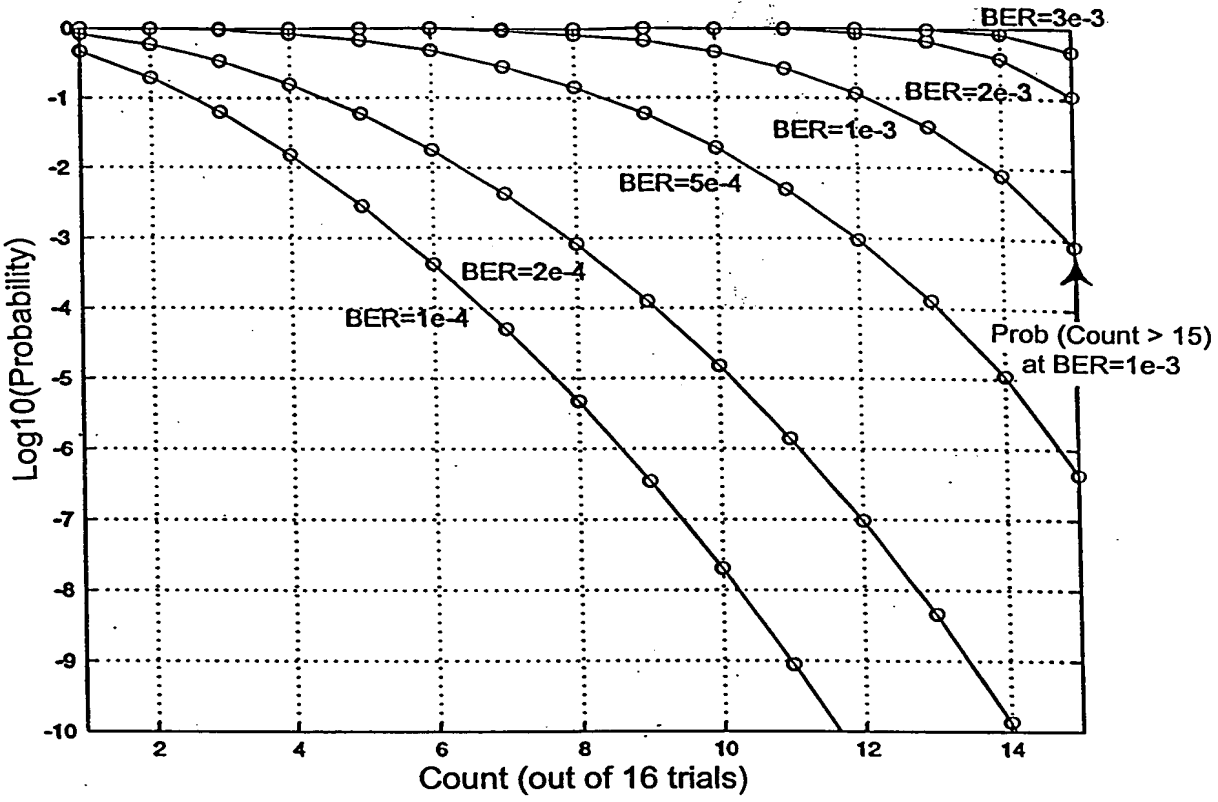

FIG. 24A

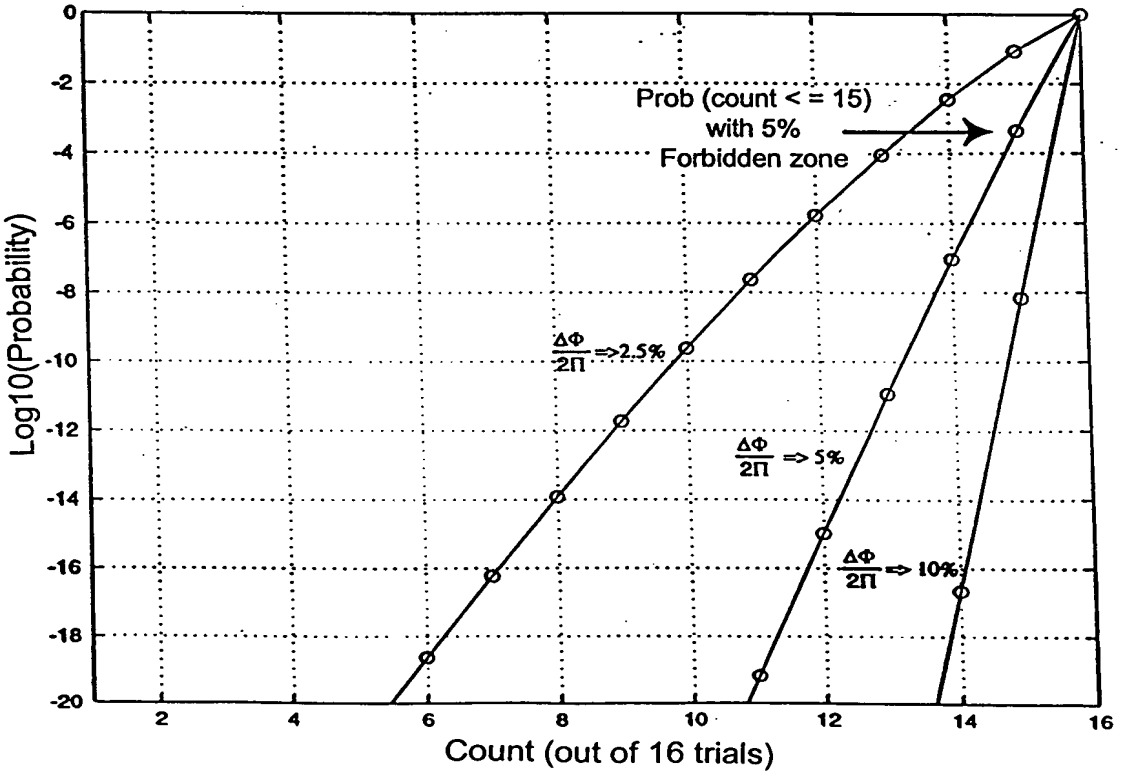

FIG. 24B

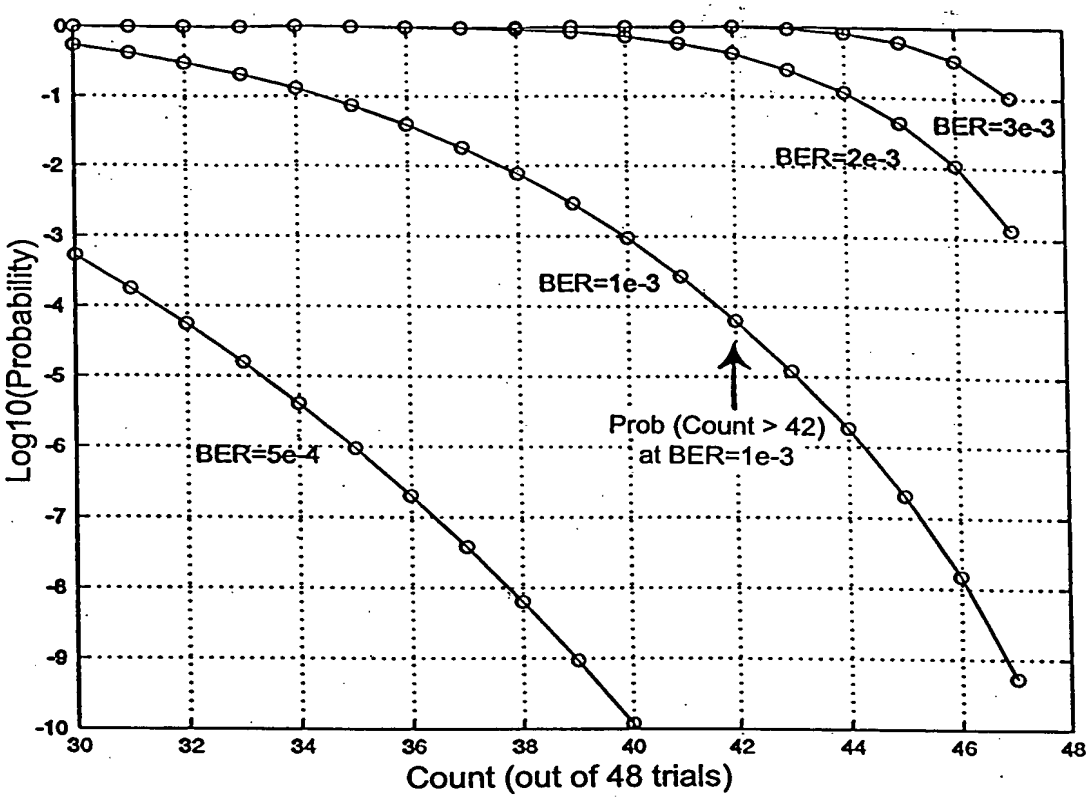

FIG. 25A

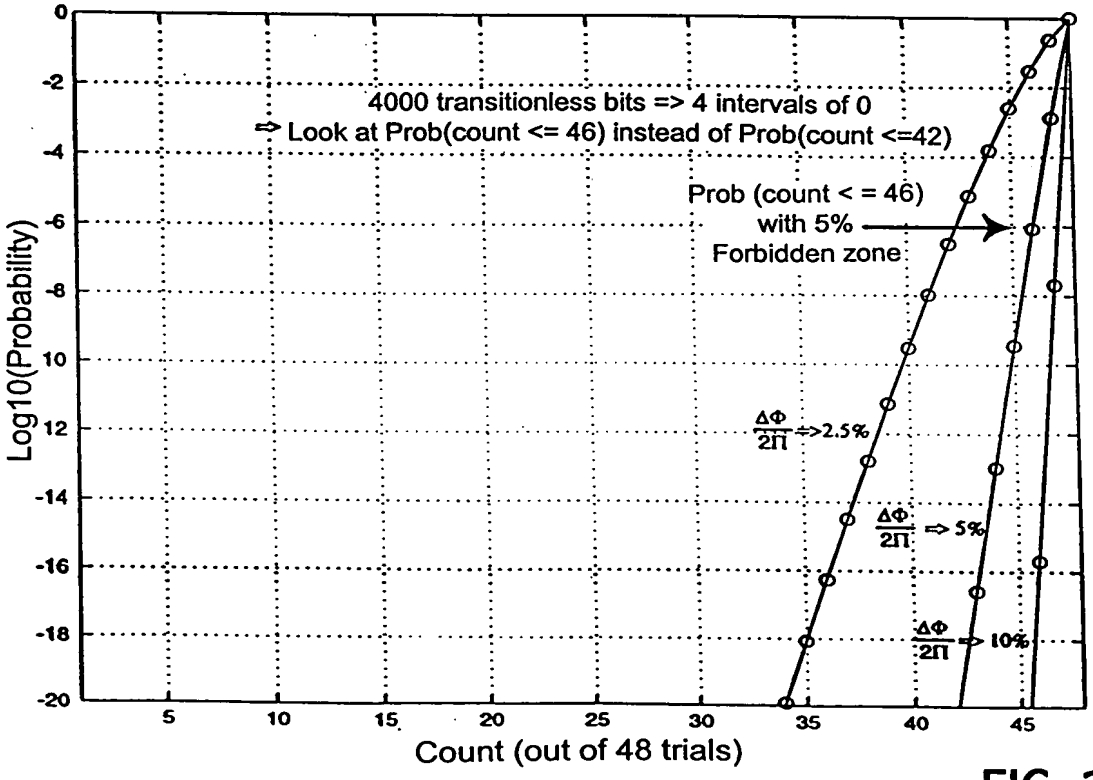

FIG. 25B

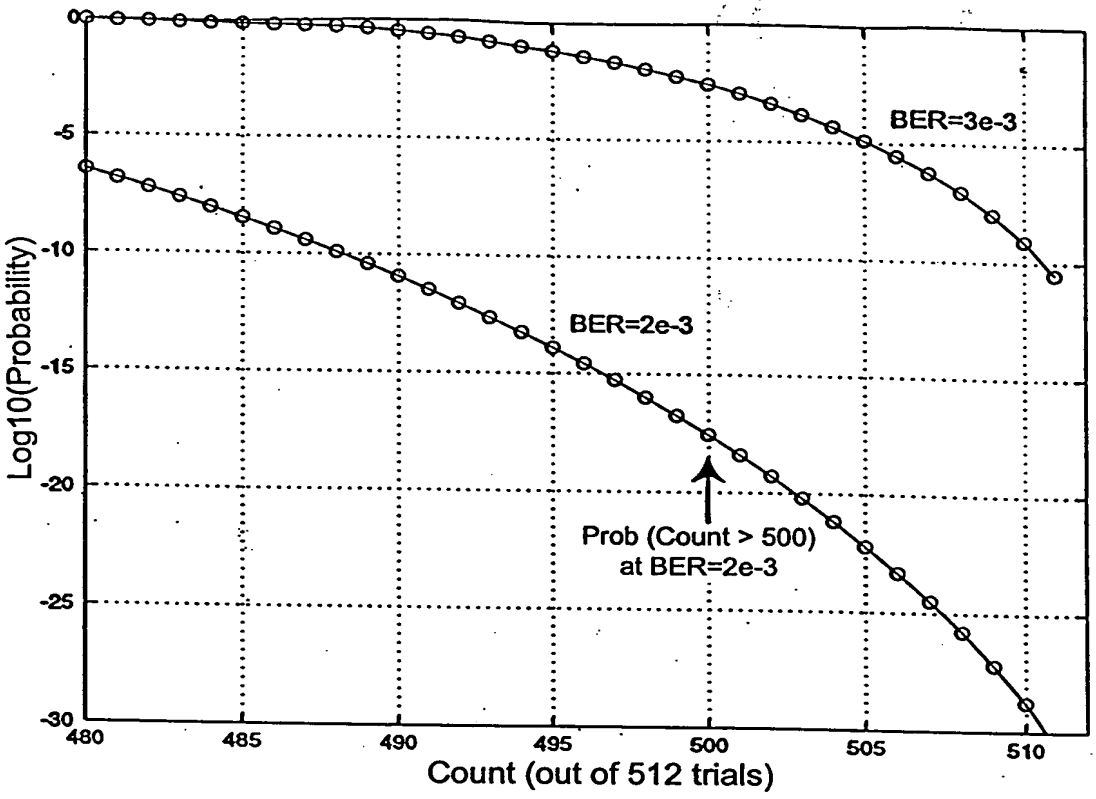

FIG. 26A

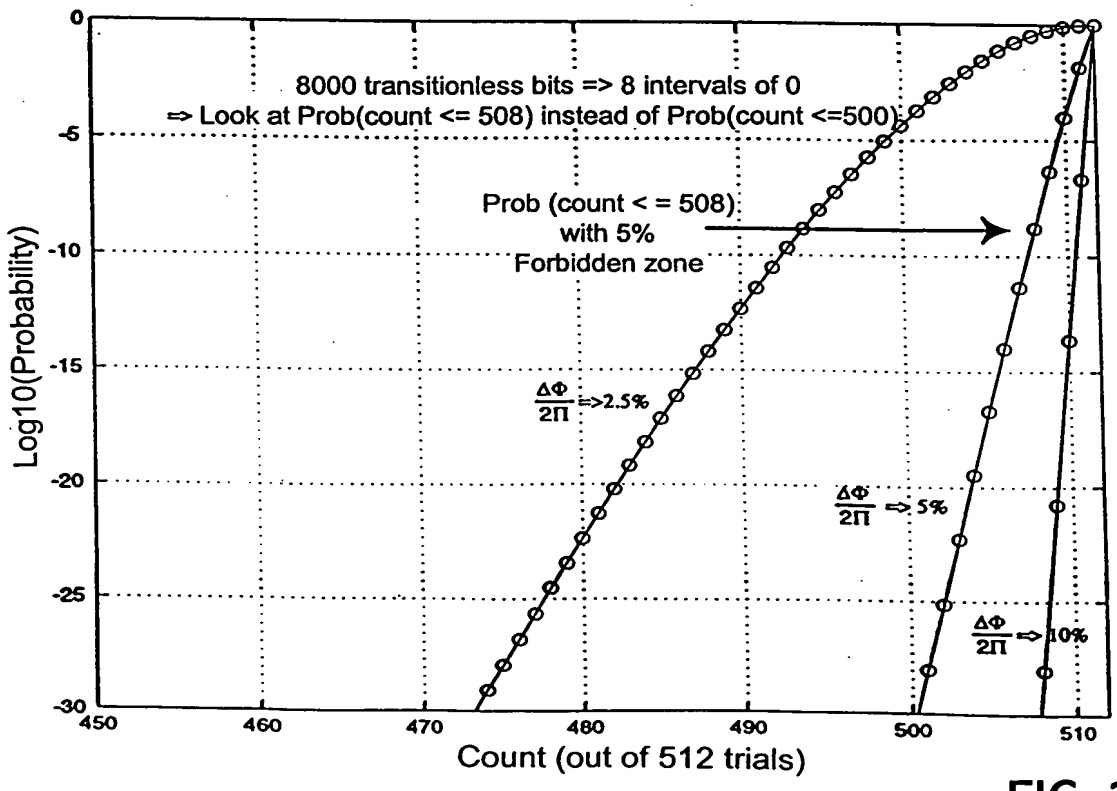

FIG. 26B

BER Counter	Digital Value
> 470	31
400-469	30
335-399	29
280-334	28
230-279	27
180-229	26
135-179	25
95-134	24
64-94	23
46-63	22
33-45	21
22-32	20
16-21	19
11-15	18
7-10	17
5-6	16
4	15
3	14
2	13
1	Use SubBER

FIG. 27A

SubBER Counter	Digital Value
> 200	12
150-199	11
100-149	10
65-99	9
34-64	8
18-33	7
10-17	6
6-9	5
4-5	4
3	3
2	2
1	1

FIG. 27B

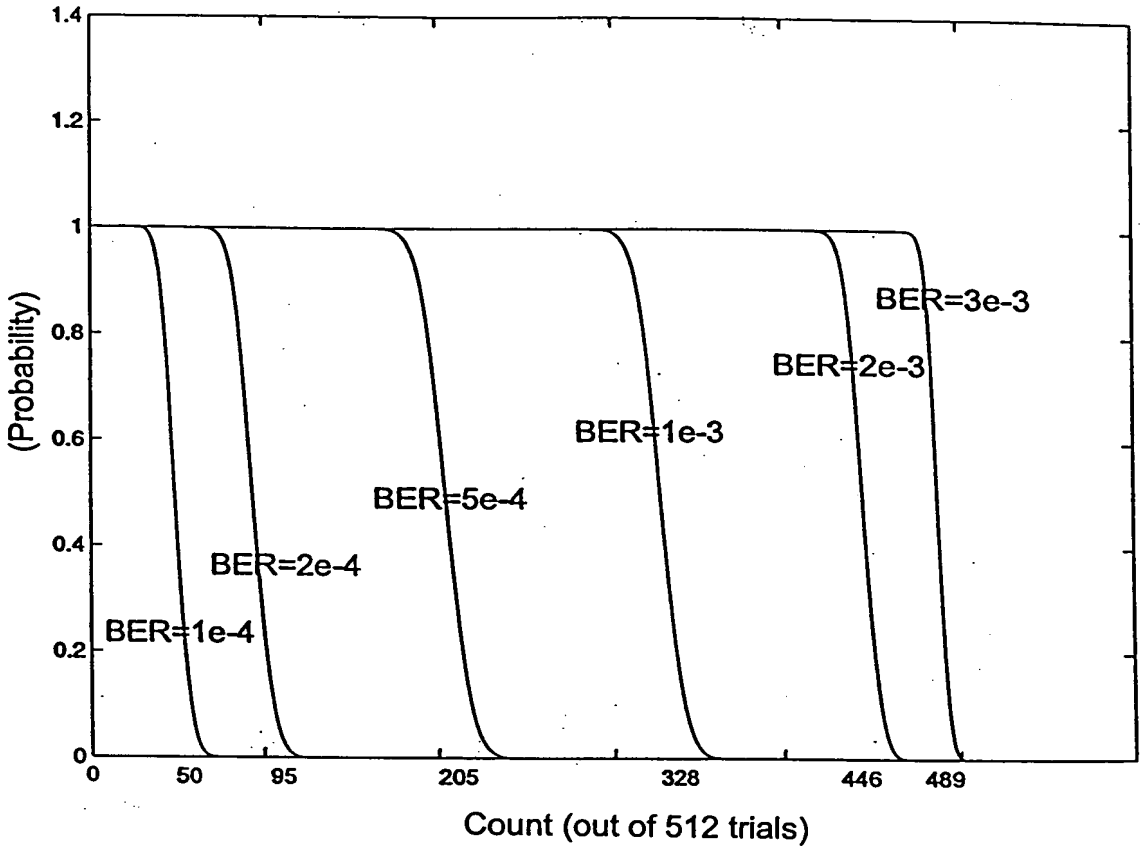
1.4
1.2
1
0.8
0.6
0.4
0.2
0
(Probability)
BER=3e-3
BER=2e-3
BER=1e-3
BER=5e-4
BER=2e-4
BER=1e-4
0
50
95
205
328
446
489
Count (out of 512 trials)

FIG. 28

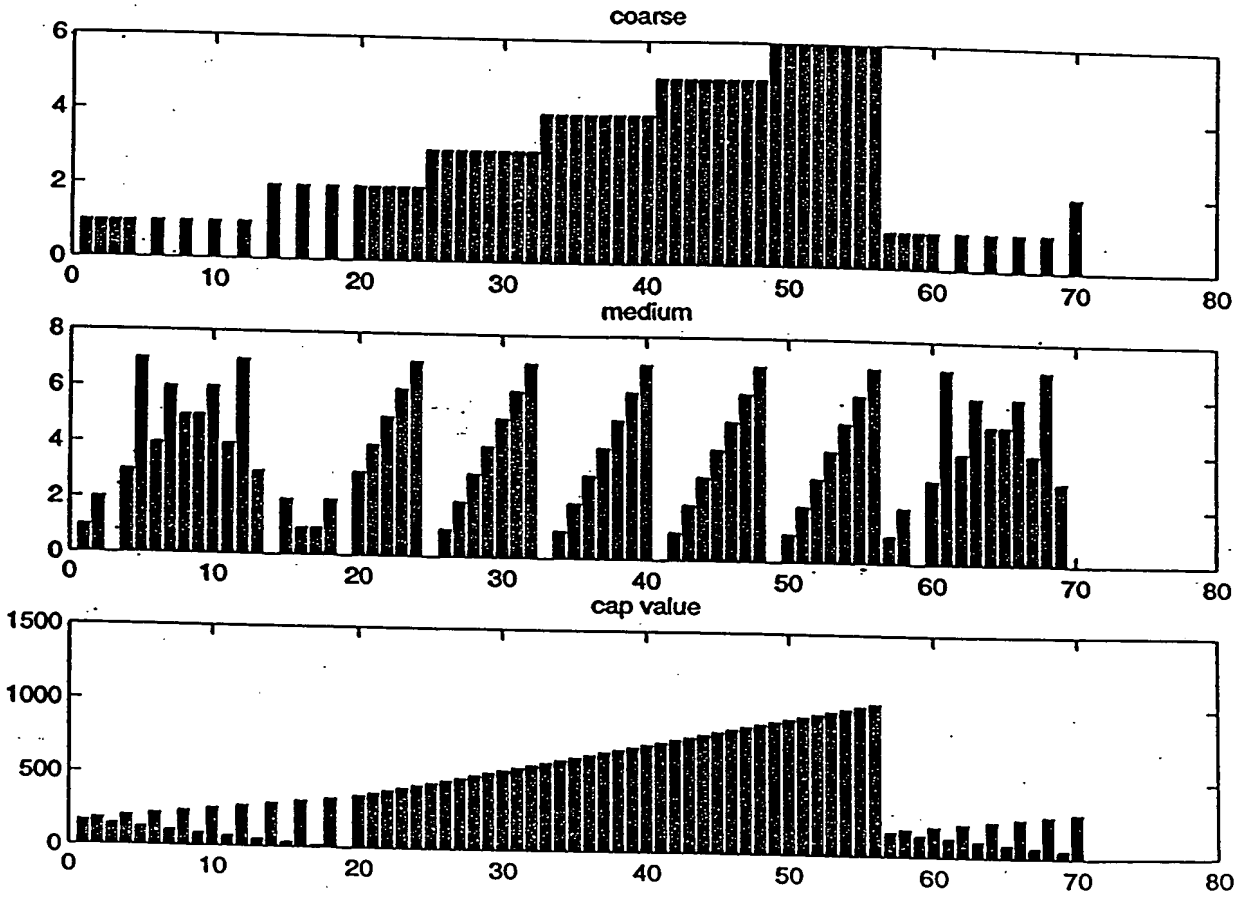
coarse
6
4
2
0
0
10
20
30
40
50
60
70
80
medium
8
6
4
2
0
0
10
20
30
40
50
60
70
80
cap value
1500
1000
500
0
0
10
20
30
40
50
60
70
80

FIG. 29

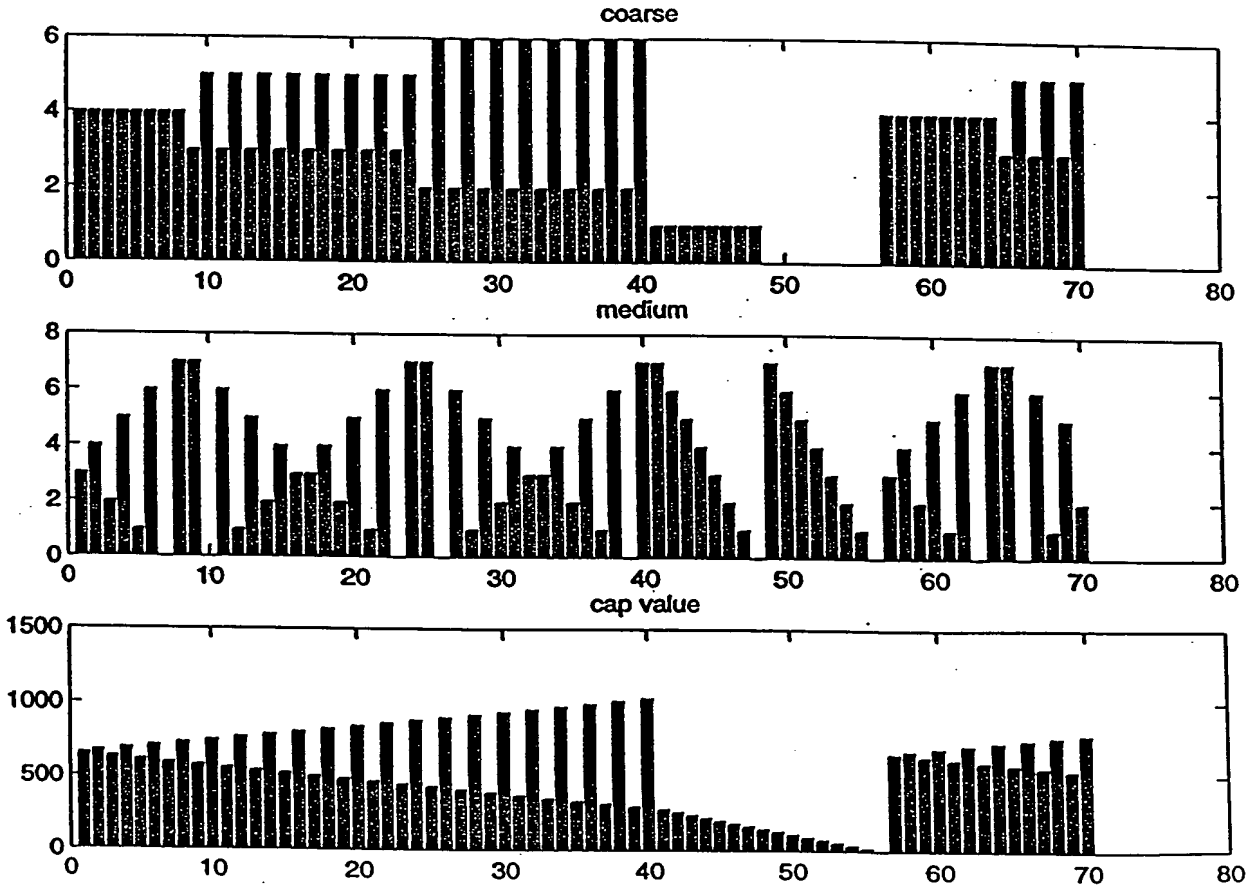
coarse
6
4
2
0
0
10
20
30
40
50
60
70
80
medium
8
6
4
2
0
0
10
20
30
40
50
60
70
80
cap value
1500
1000
500
0
0
10
20
30
40
50
60
70
80

FIG. 30

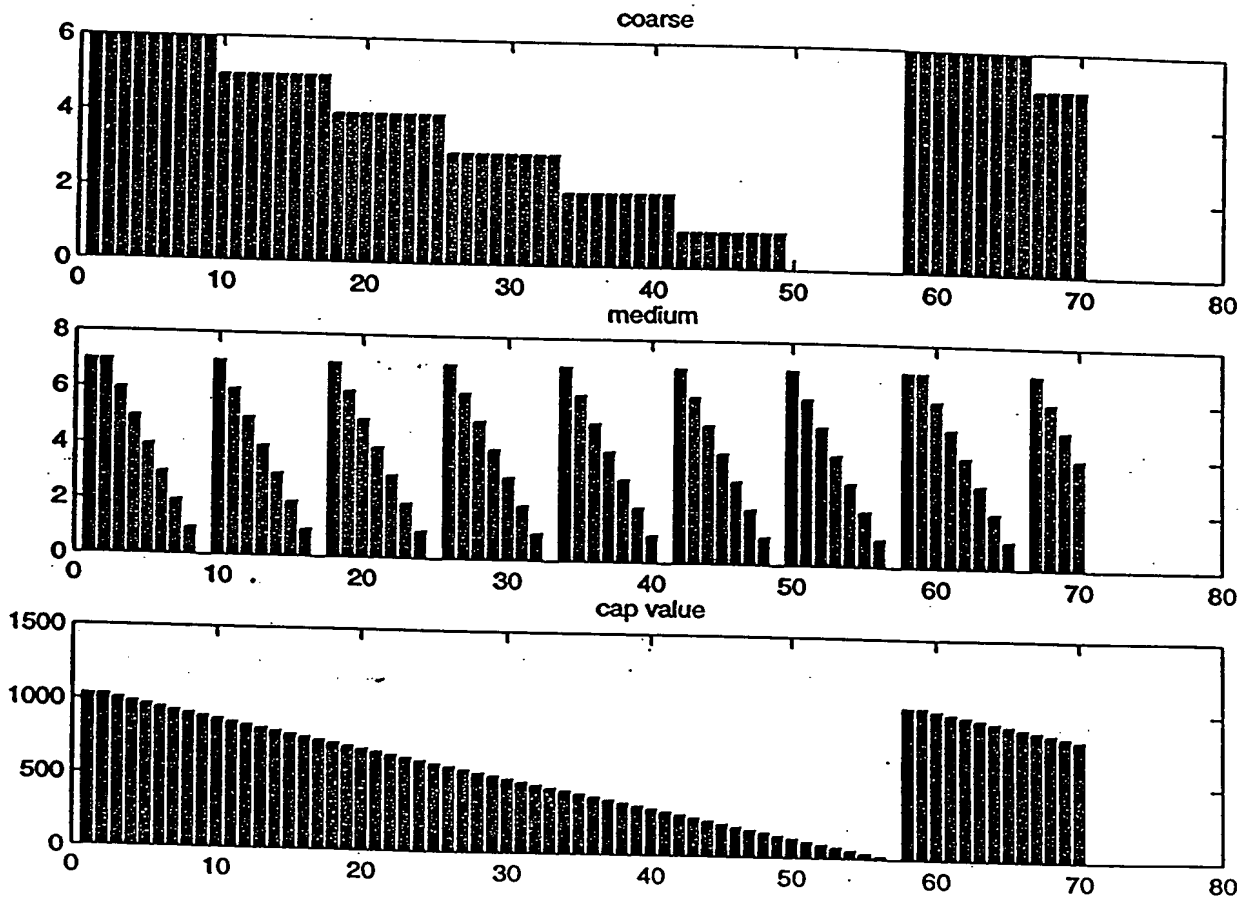
coarse
6
4
2
0
0
10
20
30
40
50
60
70
80
medium
8
6
4
2
0
0
10
20
30
40
50
60
70
80
cap value
1500
1000
500
0
0
10
20
30
40
50
60
70
80

FIG. 31

- Jitter: 0 UI
- Transition density: 1/2

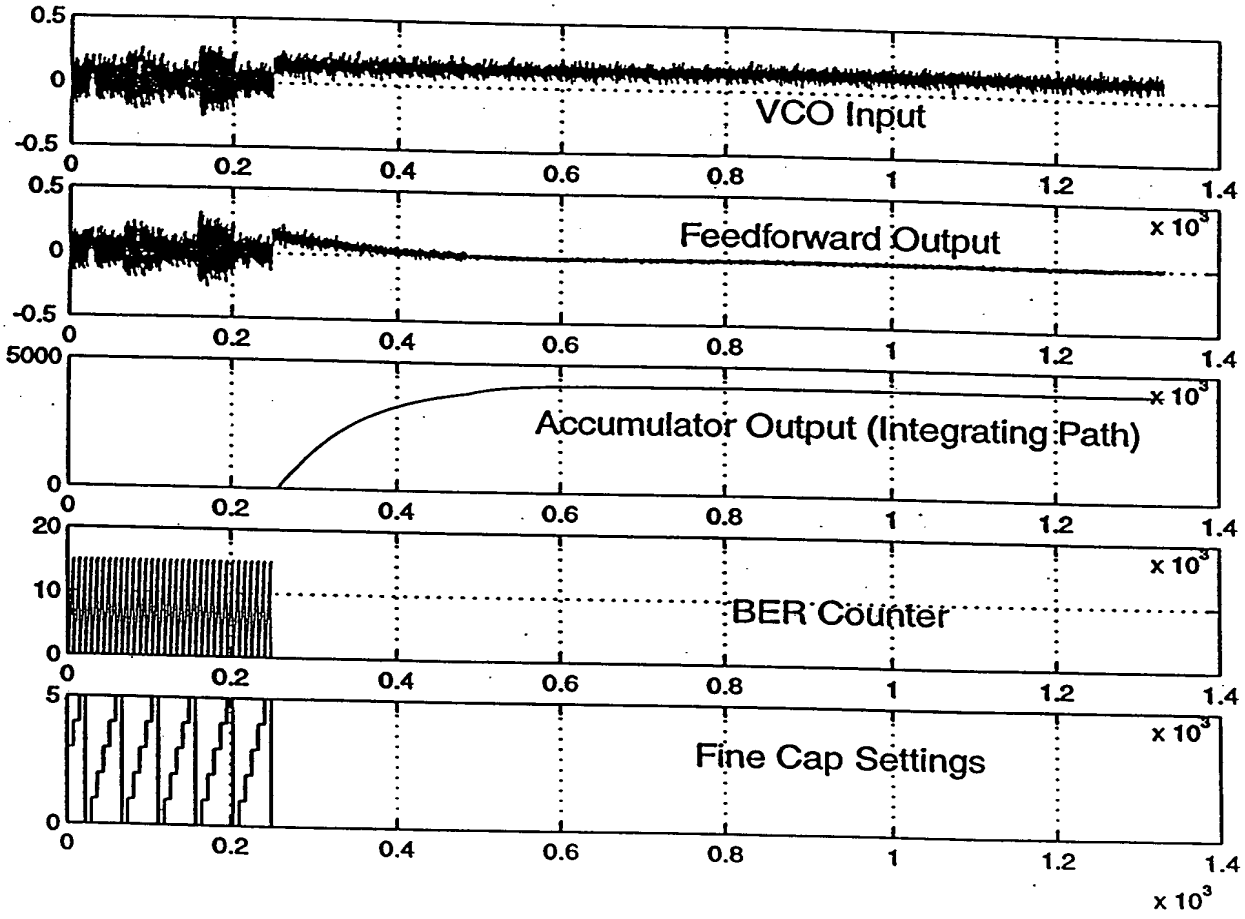

FIG. 32

- Jitter: 5 UI, 100 kHz
- Transition density: 1/2

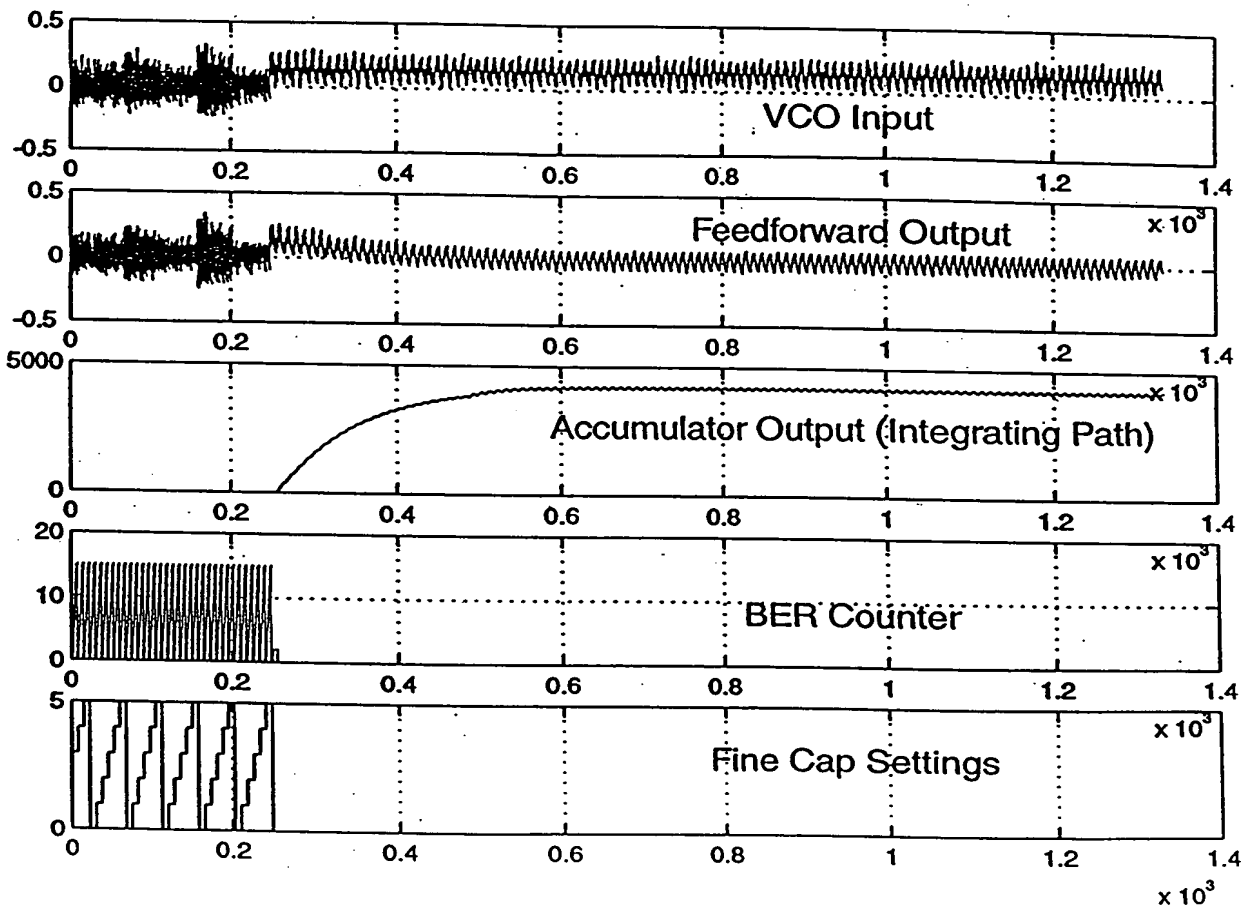

FIG. 33

- Jitter: .5 UI, 5 MHz
- Transition density: 1/2

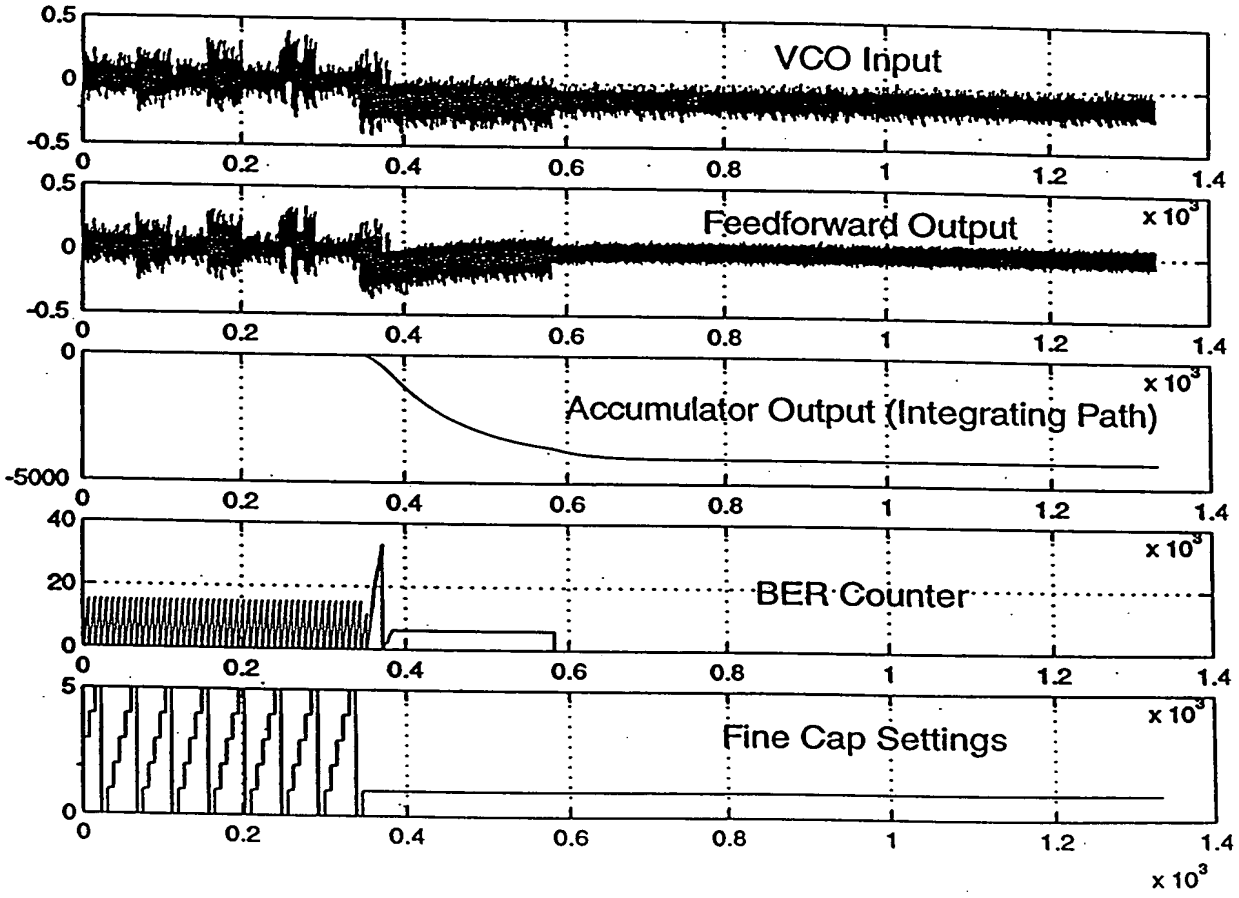

FIG. 34

- Jitter: 0 UI
- Transition density: 1/6

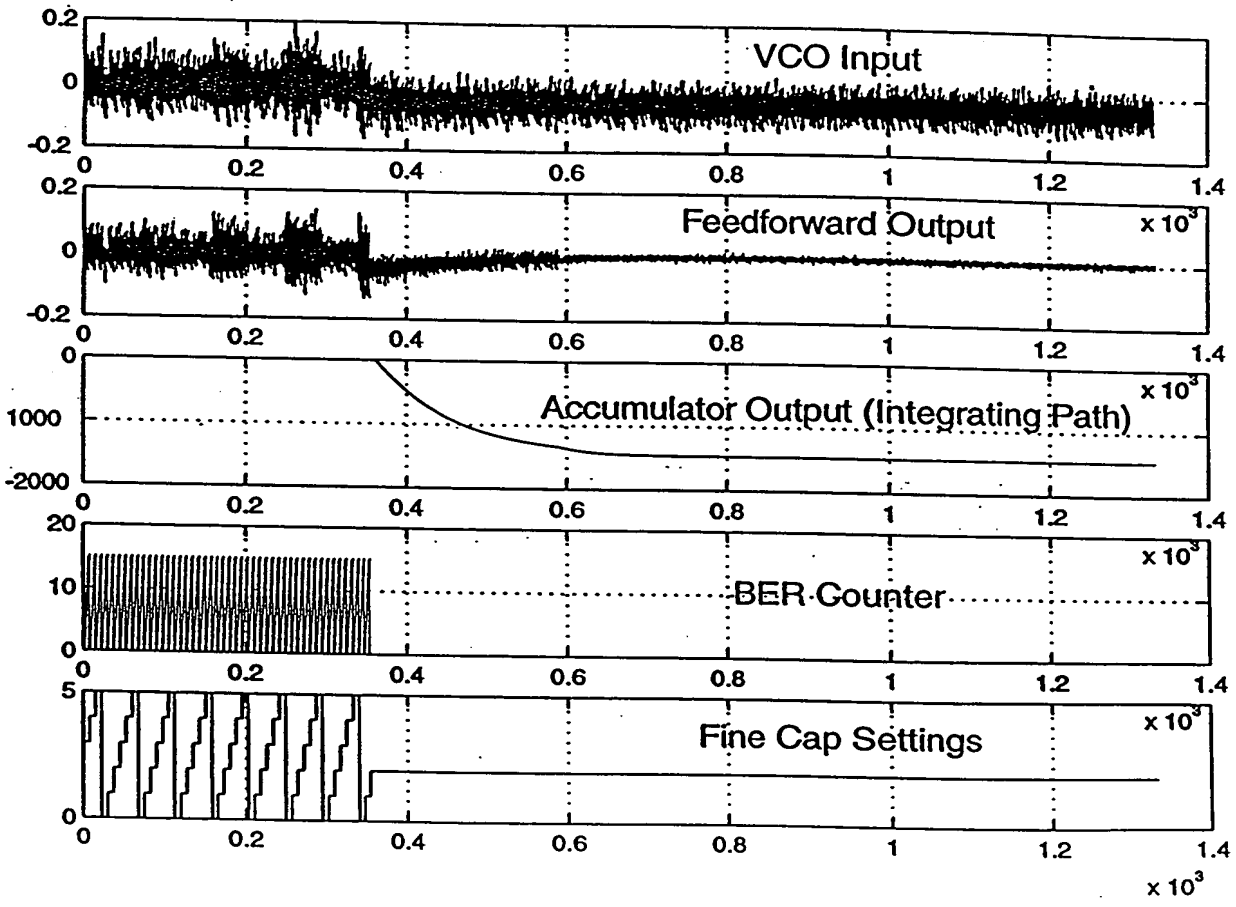

FIG. 35

- Jitter: 5 UI, 100 kHz
- Transition density: 1/6

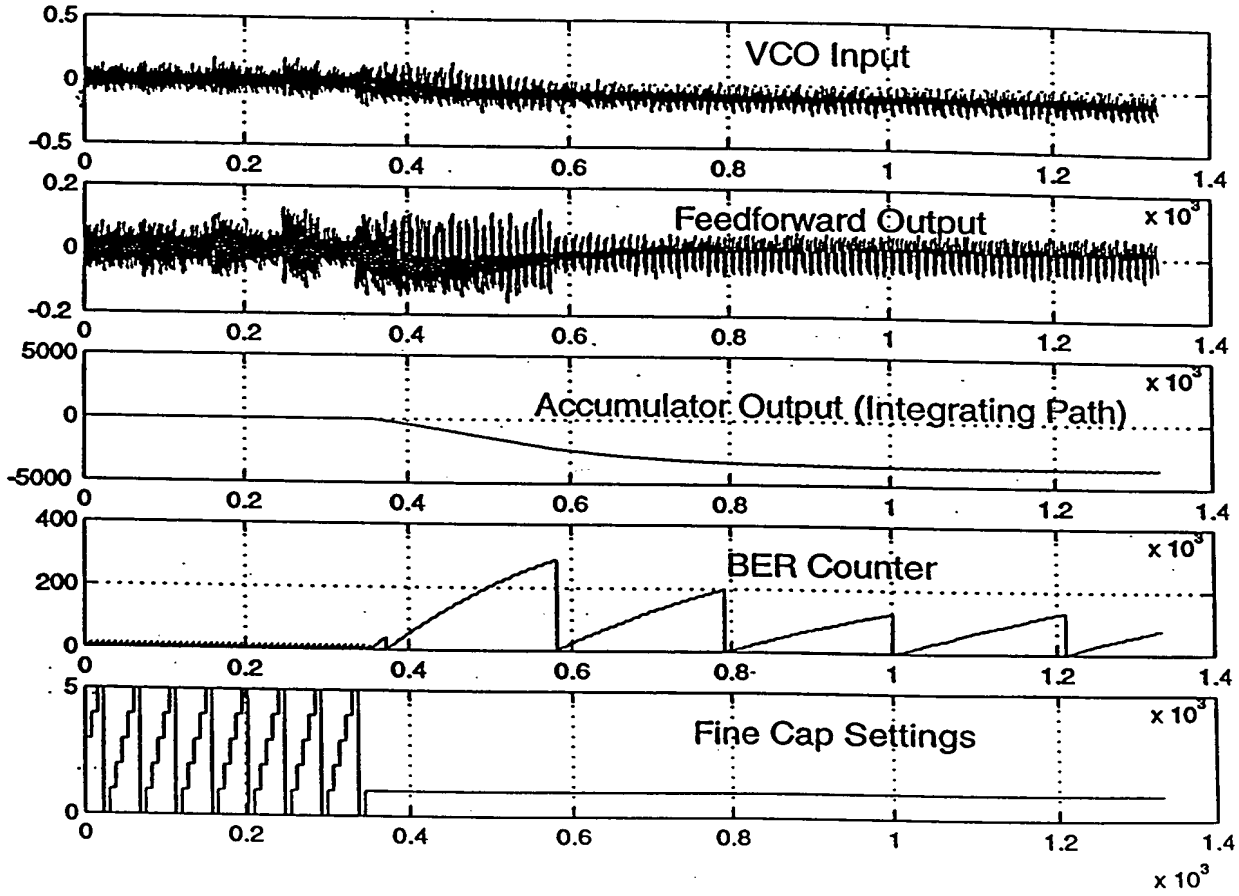

FIG. 36

- Jitter: .5 UI, 5 MHz
- Transition density: 1/6

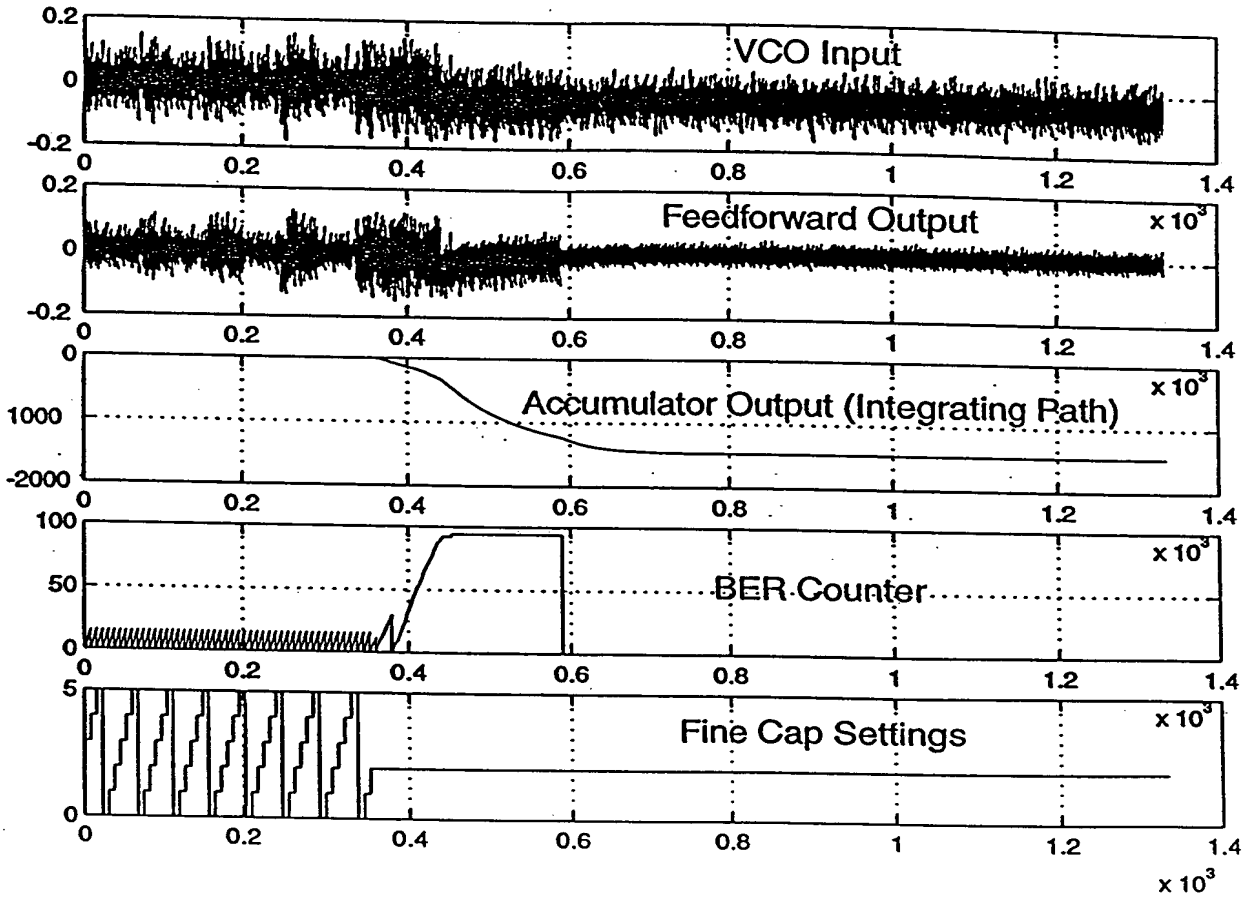

FIG. 37

- Jitter: 0 UI
- Transition density: 1

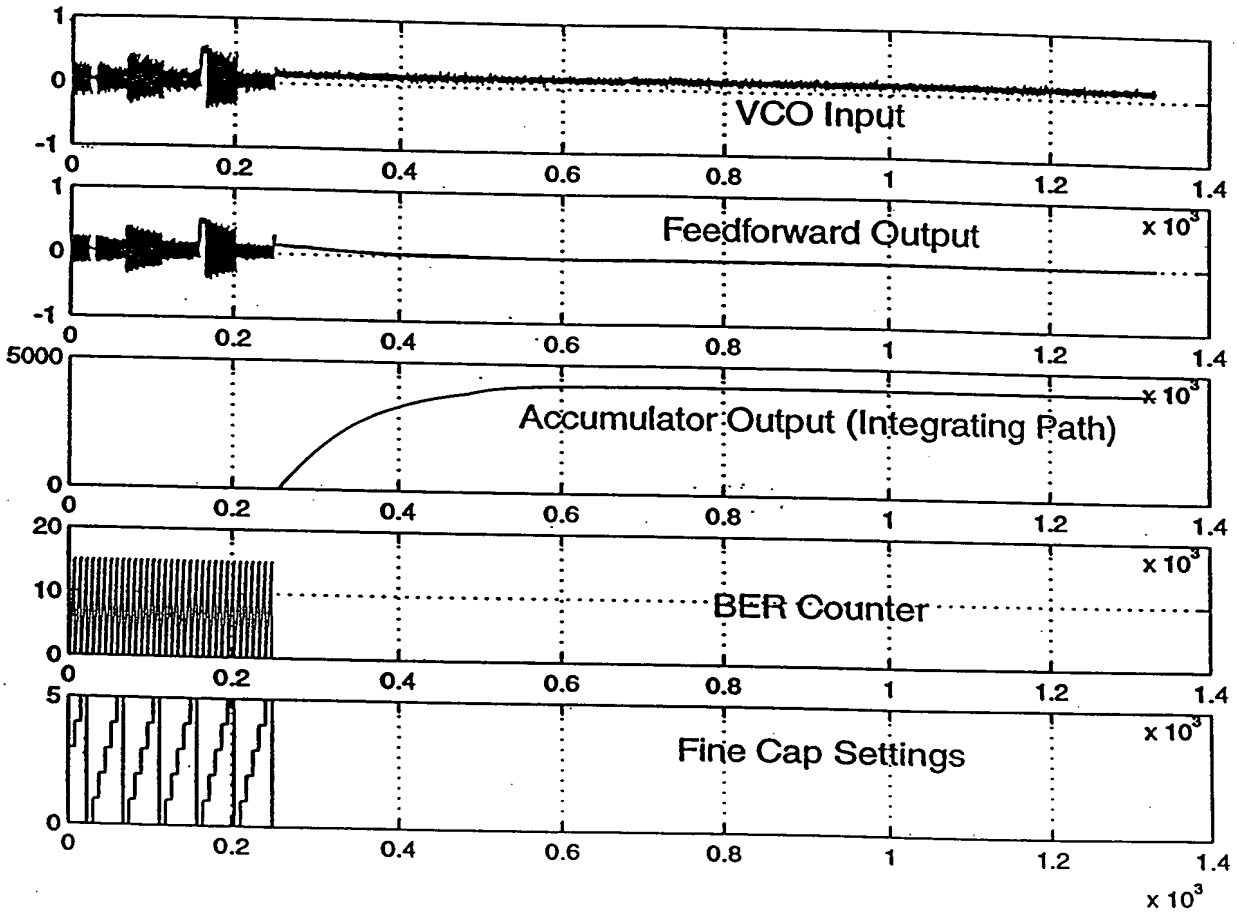

FIG. 38

- Jitter: 5 UI, 100 kHz
- Transition density: 1

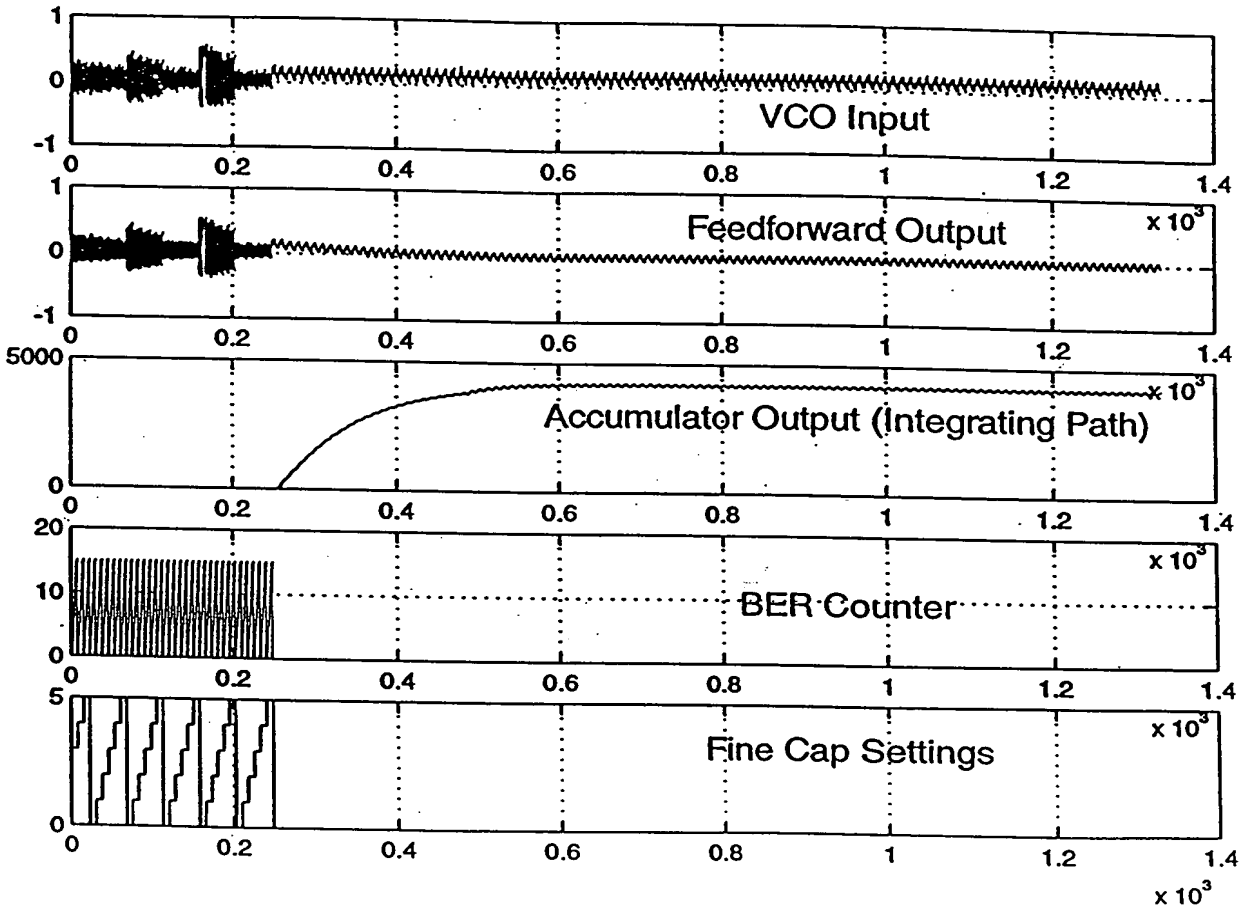

FIG. 39

- Jitter: .5 UI, 5 MHz
- Transition density: 1

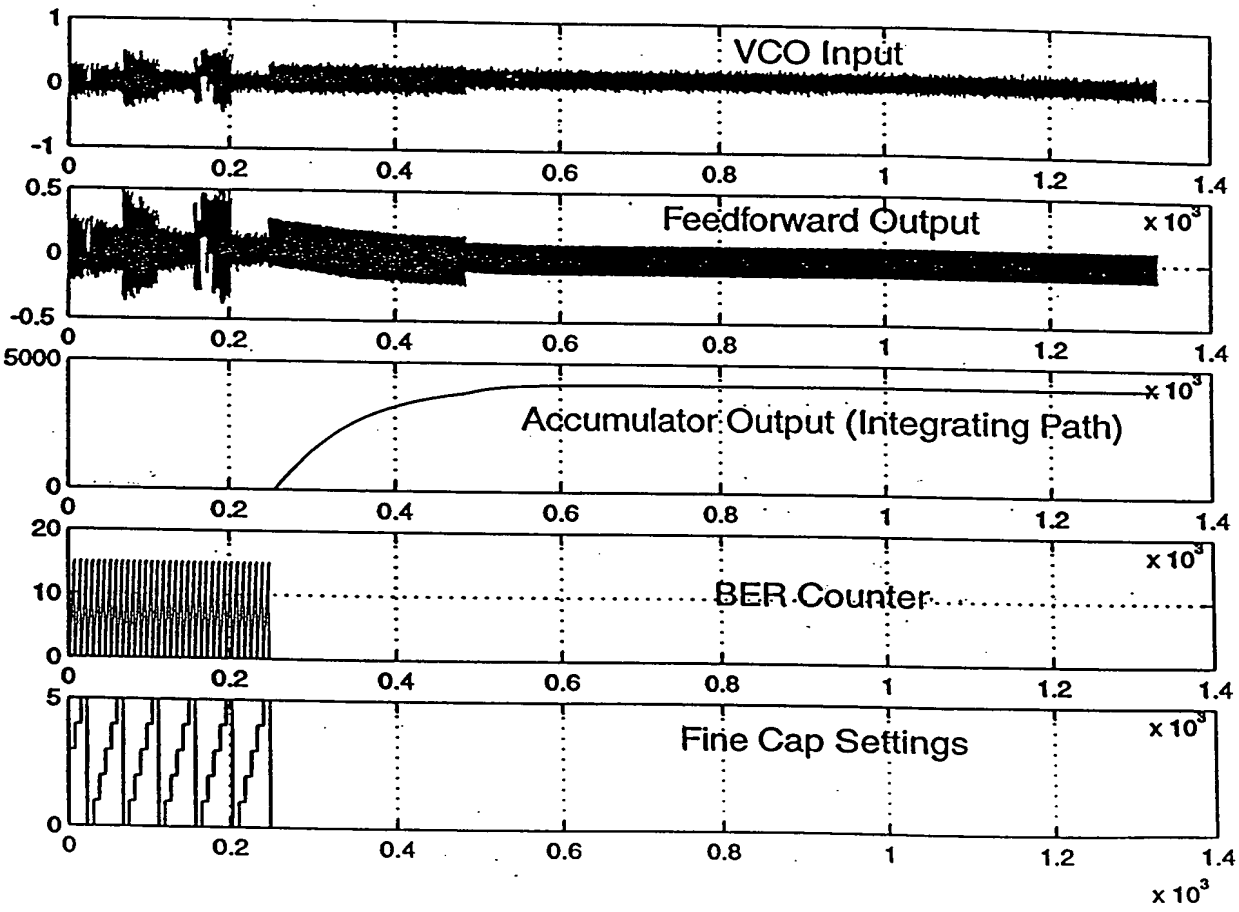

FIG. 40

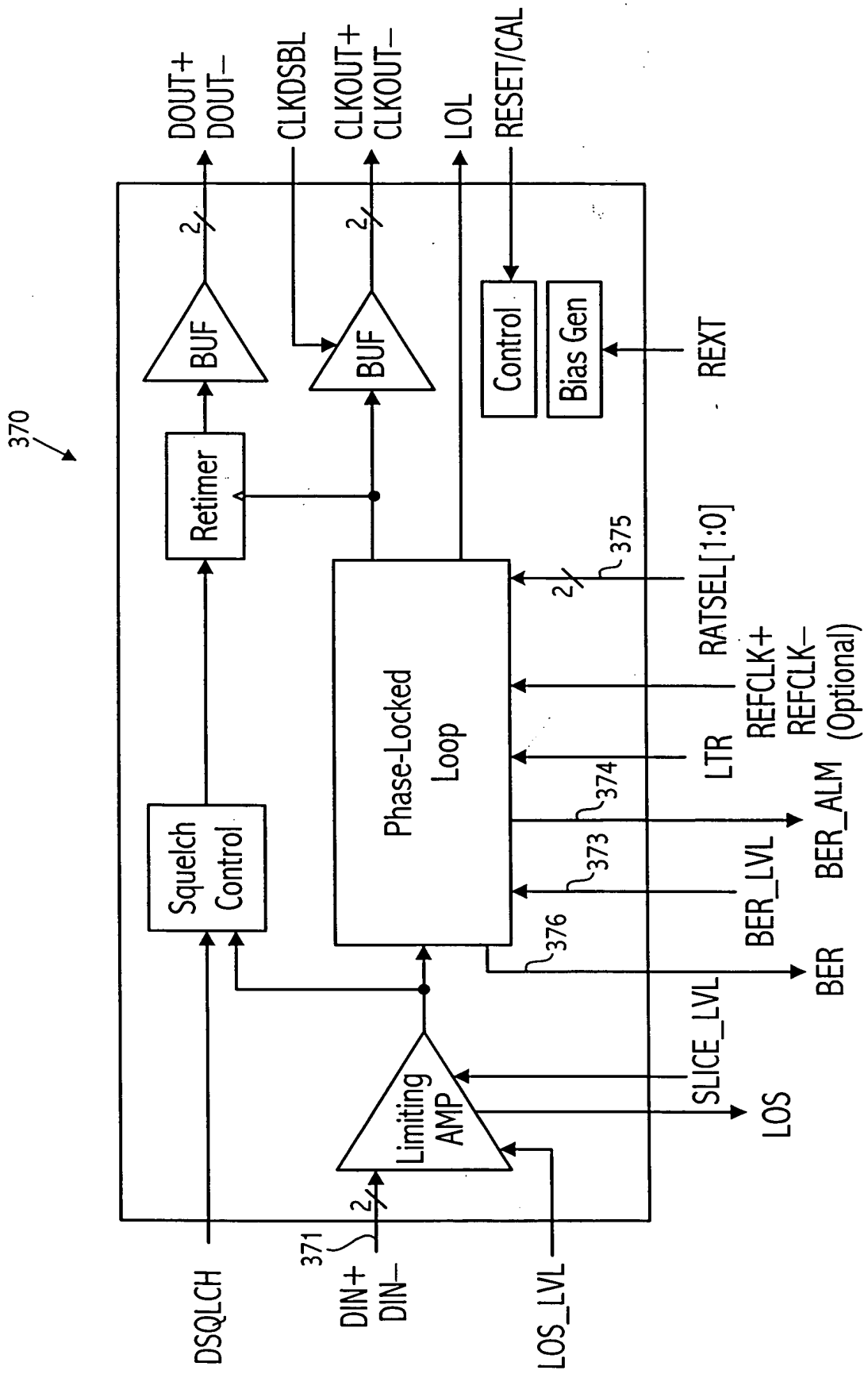
370
DOUT+
DOUT–
CLKDSBL
CLKOUT+
CLKOUT–
LOL
RESET/CAL
2
BUF
BUF
Control
Bias Gen
REXT
Retimer
375
RATSEL[1:0]
Phase-Locked Loop
LTR
REFCLK+
REFCLK–
(Optional)
374
BER_ALM
373
BER_LVL
376
BER
Squelch Control
SLICE_LVL
Limiting AMP
LOS
371
DIN+
DIN–
DSQLCH
LOS_LVL

FIG. 41